5970 Prototyping Card

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IMPORTANT!

Please read before installing your product.

Octagon's products are designed to be high in performance while consuming very little power. In order to maintain this advantage, CMOS circuitry is used.

CMOS chips have specific needs and some special requirements that the user must be aware of. Read the following to help avoid damage to your card from the use of CMOS chips.

Using CMOS Circuitry in Industrial Control

Industrial computers originally used LSTTL circuits. Because many PC components are used in laptop computers, IC manufacturers are exclusively using CMOS technology. Both TTL and CMOS have failure mechanisms, but they are different. This section describes some of the common failures which are common to all manufacturers of CMOS equipment. However, much of the information has been put in the context of the Micro PC.

Octagon has developed a reliable database of customer-induced, field failures. The average MTBF of Micro PC cards exceeds 11 years, yet there are failures. Most failures have been identified as customer-induced, but there is a small percentage that cannot be identified. As expected, virtually all the failures occur when bringing up the first system. On subsequent systems, the failure rate drops dramatically.

- Approximately 20% of the returned cards are problem-free. These cards, typically, have the wrong jumper settings or the customer has problems with the software. This causes frustration for the customer and incurs a testing charge from Octagon.

- Of the remaining 80% of the cards, 90% of these cards fail due to customer misuse and accident. Customers often cannot pinpoint the cause of the misuse.

- Therefore, 72% of the returned cards are damaged through some type of misuse. Of the remaining 8%, Octagon is unable to determine the cause of the failure and repairs these cards at no charge if they are under warranty.

The most common failures on CPU cards are over voltage of the power supply, static discharge, and damage to the serial and parallel ports. On expansion cards, the most common failures are static discharge, over voltage of inputs, over current of outputs, and misuse of the CMOS circuitry with regards to power supply sequencing. In the case of the video cards, the most common failure is to miswire the card to the flat panel display. Miswiring can damage both the card and an expensive display.

- **Multiple component failures** - The chance of a random component failure is very rare since the average MTBF of an Octagon card is greater than 11 years. In a 7 year study,

Octagon has never found a single case where multiple IC failures were not caused by misuse or accident. It is very probable that multiple component failures indicate that they were user-induced.

- **Testing "dead" cards** - For a card that is "completely nonfunctional", there is a simple test to determine accidental over voltage, reverse voltage or other "forced" current situations. Unplug the card from the bus and remove all cables. Using an ordinary digital ohmmeter on the 2,000 ohm scale, measure the resistance between power and ground. Record this number. Reverse the ohmmeter leads and measure the resistance again. If the ratio of the resistances is 2:1 or greater, fault conditions most likely have occurred. A common cause is miswiring the power supply.

- **Improper power causes catastrophic failure** - If a card has had reverse polarity or high voltage applied, replacing a failed component is not an adequate fix. Other components probably have been partially damaged or a failure mechanism has been induced. Therefore, a failure will probably occur in the future. For such cards, Octagon highly recommends that these cards be replaced.

- **Other over-voltage symptoms** - In over-voltage situations, the programmable logic devices, EPROMs and CPU chips, usually fail in this order. The failed device may be hot to the touch. It is usually the case that only one IC will be overheated at a time.

- **Power sequencing** - The major failure of I/O chips is caused by the external application of input voltage while the Micro PC power is off. If you apply 5V to the input of a TTL chip with the power off, nothing will happen. Applying a 5V input to a CMOS card will cause the current to flow through the input and out the 5V power pin. This current attempts to power up the card. Most inputs are rated at 25 mA maximum. When this is exceeded, the chip may be damaged.

- **Failure on power-up** - Even when there is not enough current to destroy an input described above, the chip may be destroyed when the power to the card is applied. This is due to the fact that the input current biases the IC so that it acts as a forward biased diode on power-up. This type of failure is typical on serial interface chips.

- **Serial and parallel** - Customers sometimes connect the serial and printer devices to the Micro PC while the power is off. This can cause the failure mentioned in the above section, *Failure upon power-up*. Even if they are connected with the Micro PC on, there can be another failure mechanism. Some serial and printer devices do not share the same power (AC) grounding. The leakage can cause the serial or parallel signals to be 20-40V above the Micro PC ground, thus, damaging the ports as they are plugged in. This would not be a problem if the ground pin is connected first, but there is no guarantee of this. Damage to the printer port chip will cause the serial ports to fail as they share the same chip.

- **Hot insertion** - Plugging cards into the card cage with the power on will usually not cause a problem. (**Octagon urges that you do not do this!**) However, the card may be damaged if the right sequence of pins contacts as the card is pushed into the socket. This usually damages bus driver chips and they may become hot when the power is applied. This is one of the most common failures of expansion cards.

- **Using desktop PC power supplies** - Occasionally, a customer will use a regular desktop PC power supply when bringing up a system. Most of these are rated at 5V at 20A or more. Switching supplies usually require a 20% load to operate properly. This means 4A or more. Since a typical Micro PC system takes less than 2A, the supply does not regulate properly. Customers have reported that the output can drift up to 7V and/or with 7-8V voltage spikes. Unless a scope is connected, you may not see these transients.

- **Terminated backplanes** - Some customers try to use Micro PC cards in backplanes that have resistor/capacitor termination networks. CMOS cards cannot be used with termination networks. Generally, the cards will function erratically or the bus drivers may fail due to excessive output currents.

- **Excessive signal lead lengths** - Another source of failure that was identified years ago at Octagon was excessive lead lengths on digital inputs. Long leads act as an antenna to pick up noise. They can also act as unterminated transmission lines. When 5V is switch onto a line, it creates a transient waveform. Octagon has seen submicrosecond pulses of 8V or more. The solution is to place a capacitor, for example 0.1 µF, across the switch contact. This will also eliminate radio frequency and other high frequency pickup.

INTRODUCTION

The 5970 prototyping card is a printed circuit card designed for creating custom circuitry for the Micro PC Bus. It contains data bus buffers, address bus buffers and 10–bit I/O decoding circuitry. Decoding is provided to select 4 of 8 or 8 of 8 chip select lines. An iSBX connector allows you to expand 5970 functionality by plugging in specialized modules.

OPERATION

Buffering

The 5970's data bus buffer provides buffering and direction control for data bus signals D0–D7. This buffer is turned on for an entire group of addresses as determined by W1 and W2 jumpers. When adding other expandable cards, make sure they are jumpered outside the address range set by W1 and W2. For example, if W1 is configured for 8 address blocks with a base address of 100H, the 5970's bus driver will be enabled when any address within 100H–11FH is selected.

Complete buffering of the lower 8 address signals (A0–A7) is provided by the 5970's address buffers.

Decoding

Address lines A0–A9, IOR* and IOW* are decoded by the 5970 Address Decoder. A card select signal is then generated to enable on card I/O operations.

The eight separate chip select lines are decoded by the decode logic circuitry. These lines are located at the grid edge and can be jumpered to decode 4, 8 or 16 addresses per chip select line.

I/O Addressing

The 5970 is I/O mapped and can occupy 32 to 64 I/O port addresses (based on block size configuration). Base addresses are selectable from 0 to 300H.

A chip select line will go low when 1 of 4 , 1 of 8, or 1 of 16 addresses within its range is selected. The chip select can be used to interface to “intelligent” ICs such as motion controllers, serial communications, and other multifunction ICs.

An address block consists of a decoded range of addresses. When 8 address blocks are selected, a particular chip select will decode 4 addresses. When 4 address blocks are selected, a particular chip select will decode 8 or 16 addresses.

W1 selects the base address and offset of the card. W2 configures the 5970 for 4 or 8 address blocks and 4, 8, or 16 address lines per each block.

Grid Area

The 5970 provides a 2.2" x 4.7" grid area with plated through holes for 0.025" posts on 0.1" centers. The grid area is designed to accommodate wire–wrap posts and your customized circuitry. The address, data, and control signals are available at the grid edge.

iSBX Interface Connector

The I/O capabilities of the 5970 can be customized using the iSBX interface. This interface accommodates on single–wide, 36–pin (8–bit) I/O expansion modules that mount directly to the 5970. The iSBX standard is supported by numerous manufacturers who offer expansion modules for A/D and D/A conversions, calendar clock functions, etc. Refer to “**CONNECTOR PINOUTS**” for a connector pinout table.

JUMPER INFORMATION

W1— Base Address Select:

The following table shows the mapping options for selecting the 5970 base address:

W1: Base Address Select		
A9	**A8**	**Base Address**
[11-12]	[9-10]	000H
[11-12]	Not jumpered	100H
Not jumpered	[9-10]	200H
Not jumpered	Not jumpered	300H

W1: Offset Address Select (4 Addresses per Chip Select)

The following table shows the offset addresses available for mapping the 5970. In this configuration the 5970 occupies 32 addresses and supports 8 chip select lines. Each chip select line has 4 addresses. A chip select line goes low when any 1 of its 4 addresses is selected. Before setting offset jumpers, make sure W2 [7–8], [13–14], and [19–20] jumpers are installed.

W1: Offset Address Select (4 Addresses per Chip Select)											
A7	**A6**	**A5**	**BA5**	**CS0**	**CS1**	**CS2**	**CS3**	**CS4**	**CS5**	**CS6**	**CS7**
[7-8]	[5-6]	[3-4]	[1-2]	0-3H	4-7H	8-BH	C-FH	10-13H	14-17H	18-1BH	1C-1FH
[7-8]	[5-6]	NJ	[1-2]	20-23H	24-27H	28-2BH	20-2FH	30-33H	34-37H	38-3BH	3C-3FH
[7-8]	NJ	[3-4]	[1-2]	40-43H	44-47H	48-4BH	4C-4FH	50-53H	54-57H	58-5BH	5C-5FH
[7-8]	NJ	NJ	[1-2]	60-63H	64-67H	68-6BH	6C-6FH	70-73H	74-77H	78-7BH	7C-7FH
NJ	[5-6]	[3-4]	[1-2]	80-83H	84-87H	88-8BH	8C-8FH	90-93H	94-97H	98-9BH	9C-9FH
NJ	[5-6]	NJ	[1-2]	A0-A3H	A4-A7H	A8-ABH	AC-AFH	B0-B3H	B4-B7H	B8-BBH	BC-BFH
NJ	NJ	[3-4]	[1-2]	C0-C3H	C4-C7H	C8-CBH	CC-CFH	D0-D3H	D4-D7H	D8-DBH	DC-DF
NJ	NJ	NJ	[1-2]	E0-E3H	E4-E7H	E8-EBH	EC-EFH	F0-F3H	F4-F7H	F8-FBH	FC-FFH

W1: Offset Address Select (8 Addresses per Chip Select)

The following table shows the offset addresses available for mapping the 5970. In this configuration the 5970 occupies 64 addresses and supports 8 chip select lines. Each chip select line has 8 addresses. A chip select line goes low when any 1 of its 8 addresses is selected. Before setting offset jumpers, make sure W2 [5–6], [11–12], and [17–18] jumpers are installed.

W1: Offset Address Select (8 Addresses per Chip Select)											
A7	**A6**	**A5**	**BA5**	**CS0**	**CS1**	**CS2**	**CS3**	**CS4**	**CS5**	**CS6**	**CS7**
[7-8]	[5-6]	NJ	NJ	00-07H	08-0FH	10-17H	18-1FH	20-27H	28-2FH	30-37H	38-3FH
[7-8]	NJ	NJ	NJ	40-47H	48-4FH	50-57H	58-5FH	60-67H	68-6FH	70-77H	78-7FH
NJ	[5-6]	NJ	NJ	80-87H	88-8FH	90-97H	98-9FH	A0-A7H	A8-AFH	B0-B7H	B8-BFH
NJ	NJ	NJ	NJ	C0-C7H	C8-CFH	D0-D7H	D8-DFH	E0-E7H	E8-EFH	F0-F7H	F8-FFH

W1: Offset Address Select (16 Addresses per Chip Select)

The following table shows the offset addresses available for mapping the 5970. In this configuration the 5970 occupies 64 addresses and supports 4 chip select lines. Each chip select line has 16 addresses. A chip select line goes low when any 1 of its 16 addresses is selected. Before setting offset jumpers, make sure W2 [1–2], [9–10], and [15–16] jumpers are installed.

W1: Offset Address Select (16 Addresses per Chip Select)							
A7	**A6**	**A5**	**BA5**	**CS0**	**CS1**	**CS2**	**CS3**
[7-8]	[5-6]	NJ	NJ	00-0FH	10-1FH	20-2FH	30-3FH
[7-8]	NJ	NJ	NJ	40-4FH	50-5FH	60-6FH	70-7FH
NJ	[5-6]	NJ	NJ	80-8FH	90–9FH	A0-AFH	B0-BFH
NJ	NJ	NJ	NJ	C0-CFH	D0-DFH	E0-EFH	F0-FFH

W2: Address Block Size

The following table shows jumper options for configuring the 5970 for 4 or 8 address blocks. An address block is a collection of address lines. The number of address lines in each block (per chip select) is indicated below:

W2: Address Block Size	
Pins Jumpered	**Description**
[5-6] [11-12] [17-18]	Each input and output strobe line occupies 4 address blocks with 8 addresses per chip select
[1-2] [9-10] [15-16]	Each input and output strobe line occupies 4 address blocks with 16 addresses per chip select
[7-8] [13-14] [19-20]	Each input and output strobe line occupies 8 address blocks with 4 addresses per chip select

W3: Interrupt Level Select

Selects any 2 (INT0 & INT1) of 6 (IRQ2 – IRQ7) interrupt requests from PC Bus to iSBX connector and prototyping area.

W4: DMA Channel Select:

This jumper can select 1 of 3 DMA requests (DMARQ) on the iSBX connector:

W4: DMA Channel Select	
Pins Jumpered	**DMA Request**
[5-6]	DRQ1
[3-4]	DRQ2
[1-2]	DRQ3

W: DMA Acknowledge Select:

W4 also configures the 5970 for 1 of 3 DMA acknowledge (DMACK) signals from the PC Bus to the iSBX connector.

W4: DMA Acknowledge Select	
Pins Jumpered	**DMA Request**
[7-8]	DACK3*
[9-10]	DACK2*
[11-12]	DACK1*

*active low

CONFIGURATION EXAMPLES

The following examples illustrate how to configure the 5970 for typical prototyping applications. For additional jumper information, refer to "**JUMPER TABLES**" presented earlier.

Example 1

This scenario assumes you want to configure the 5970 so it resides at base address 100H and will accommodate one 8255 IC.

1. Set the base address of the 5970 to 100H by removing W1 [9–10] and installing W1 [11–12].

2. Since the 8255 requires 4 addresses for operation, we will configure the 5970 to support 4 addresses per chip select. Install W1 [1–2], [3–4], [5–6], and [7–8] jumpers.

3. Set the decode block size to match the number of address lines required. Again, since the 8255 requires 4 address lines, we will set W2 jumpers to support this number of lines. Install W2 [7–8], [13–14], and [19–20] jumpers.

4. The 5970 is now configured to support an 8255. Hardwire the 8255 to the 5970 by connecting the following signals:

5970 Connections To 8255	
5970	**8255**
CS0	Connect to CS
A0, A1	Connect to corresponding address lines

Additional 8255 chips can be added by using the available chip select lines and the same address lines.

NOTE: If you are adding other cards on your system, make sure they reside between 120H–17FH. This avoids bus conflicts.

Example 2

This scenario assumes you want to configure the 5970 so it resides at address 140H and accommodates an intelligent serial controller chip. This chip requires 3 address lines for operation (A0, A1, and A2), a chip select line, and other lines necessary for operation.

1. Set the base address of the 5970 to 100H by removing W1 [9–10] and installing W1 [11–12].

2. Set the decode block size to match the number of lines required. We will configure W2 jumpers to support 8 address lines per chip select. Install W2 [5–6], [11–12], and [17–18] jumpers.

3. Set W1 jumpers to accommodate an offset of 40H (100H base address + 40H offset = 140H) Install W1 [7–8] and remove W1 [1–2], [3–4], and [5–6] jumpers. The 5970 is now configured to decode addresses from 140H to 17FH.

4. Hardwire the serial controller chip to the 5970 by connecting the following signals:

5970 Connections To Serial Controller	
5970	**Serial Controller Chip**
CS0	Connect to CS
A0-A3	Connect directly to chip
D0-D7	Connect directly to chip
BIOW,BIOR	Connect directly to chip

NOTE: Reset is active high. If you want reset active low, install an inverter in serial with the serial controller chip. If you are adding other cards on your system, make sure they reside between 100H–13FH. This avoids bus conflicts.

TECHNICAL SPECIFICATIONS

Mapping
Jumper selectable to any I/O address on 4 or 8 address blocks. Within the 10–bit I/O address range, make sure the I/O address of the 5970 does not conflict with other I/O devices in the system. Occupies 32 to 64 I/O port addresses based on block size configuration.

Grid Area
2.2" x 4.7" grid area with 0.035" plated–through holes for 0.025" posts on 0.1" centers.

Micro PC Bus Connector (62 pin)
0.100" spacing.

Power Requirements
5V ±0.25V at 8 mA typical, 28 mA maximum.

Environmental
Free–air operating temperature: –20° to +70°C.
Storage temperature: –40° to +85°C.
Operating humidity: 5 to 95% RH, noncondensing.

Size
4.5" x 4.9" (114.30 mm x 124.46 mm)

CONNECTOR PINOUTS

iSBX Connector Pinouts			
Pin #	**Signal**	**Pin #**	**Signal**
1	+12V	2	-12V
3	Gnd	4	+5V
5	RESET	6	CLK
7	A2	8	NC
9	A1	10	NC
11	A0	12	INT1
13	IWR*	14	INT0
15	IRD*	16	WAIT*
17	Gnd	18	+5V
19	D7	20	MCS1*
21	D6	22	MCS0*
23	D5	24	NC
25	D4	26	TDMA
27	D3	28	NC
29	D2	30	NC
31	D1	32	DMACK*
33	D0	34	DMARQ
35	Gnd	36	+5V

* = active low

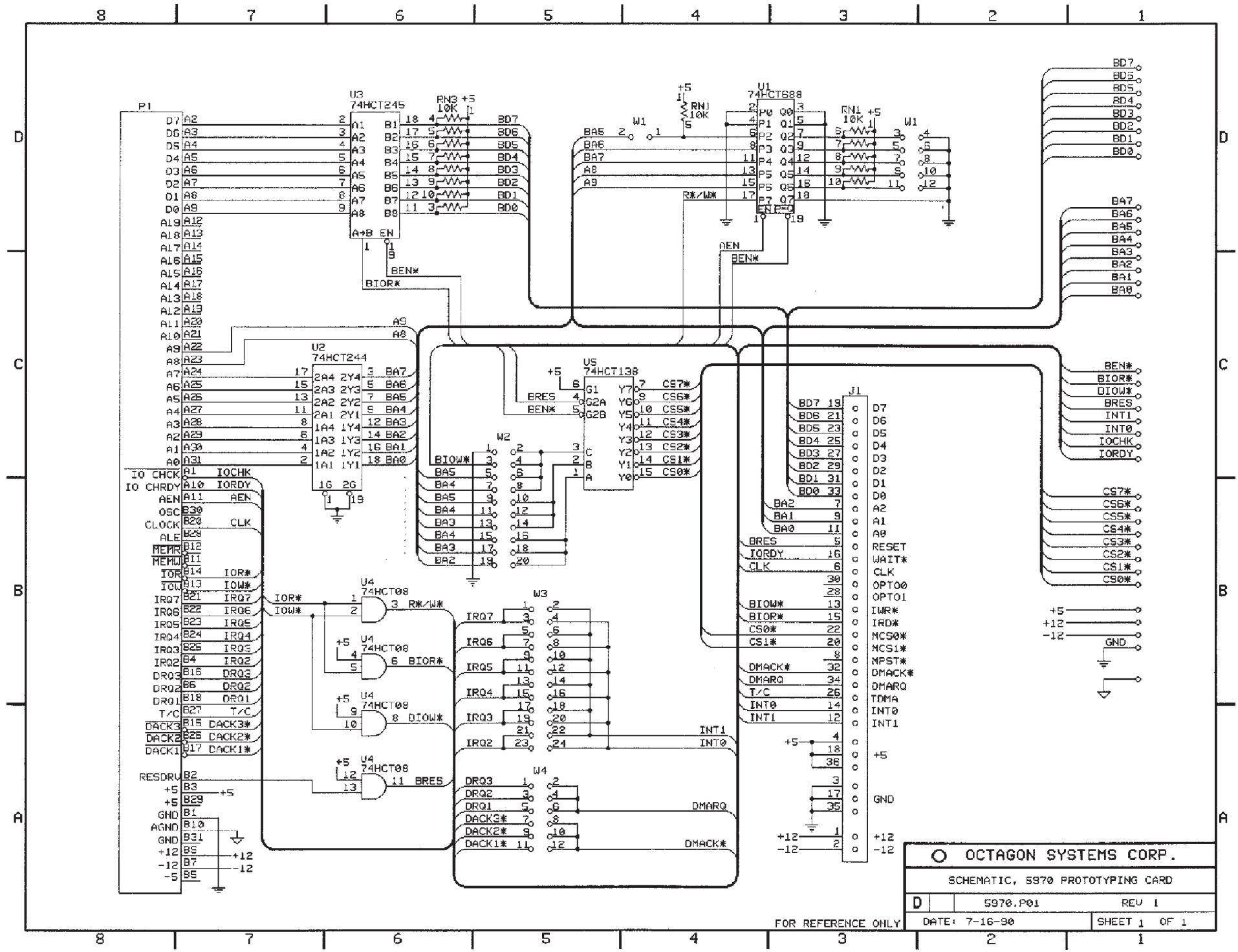
DMA channel is jumperable to channels 1, 2, or 3 to transfer data to and from the iSBX module.

Micro PC "A"					
Pin #	**Description**	**Signal**	**Pin #**	**Description**	**Signal**
A1	I/O CH CK*	I	A17	A14	O
A2	D7	I/O	A18	A13	O
A3	D6	I/O	A19	A12	O
A4	D5	I/O	A20	A11	O
A5	D4	I/O	A21	A10	O
A6	D3	I/O	A22	A9	O
A7	D2	I/O	A23	A8	O
A8	D1	I/O	A24	A7	O
A9	D0	I/O	A25	A6	O
A10	I/O CH RDY	I	A26	A5	O
A11	AEN	O	A27	A4	O
A12	A19	O	A28	A3	O
A13	A18	O	A29	A2	O
A14	A17	O	A30	A1	O
A15	A16	O	A31	A0	O
A16	A15	O			

* = active low

Micro PC "B"					
Pin #	**Description**	**Signal**	**Pin #**	**Description**	**Signal**
B1	GND	O	B17	DACKI*	O
B2	RESET	O	B18	DRQ1	I
B3	+5V	I	B19	DACK0*	O
B4	IRQ2	I	B20	CLOCK	O
B5	-5V	Not used	B21	IRQ7	I
B6	DRQ2	I	B22	IRQ6	I
B7	-12V	I	B23	IRQ5	I
B8	Reserved	Not used	B24	IRQ4	I
B9	+12V	I	B25	IRQ3	I
B10	Analog Gnd	I	B26	DACK2*	I
B11	MEMW*	O	B27	T/C	I
B12	MEMR*	O	B28	ALE	O
B13	IOW*	O	B29	Aux +5V	I
B14	IOR*	O	B30	OSC	O
B15	DACK3*	O	B31	Aux Gnd	I
B16	DRQ3	I			

* = active low


P1
U3
74HCT245
RN3 +5
10K
U1
74HCT688
RN1 +5
10K
RNJ
10K
W1
U2
74HCT244
U5
74HCT138
W2
U4
74HCT08
W3
W4
J1
BEN*
BIOR*
AEN
BRES
IOCHK
IORDY
CLK
IOR*
IOW*
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
IRQ2
DRQ3
DRQ2
DRQ1
T/C
DACK3*
DACK2*
DACK1*
RESDRV
INT1
INT0
DMARQ
DMACK*
GND
+5
+12
-12
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SCHEMATIC, 5970 PROTOTYPING CARD
5970.P01
REV 1
DATE: 7-16-90
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