Clocking HS Data Converters 101

Communications Clocking Group

Texas Instruments

Introduction

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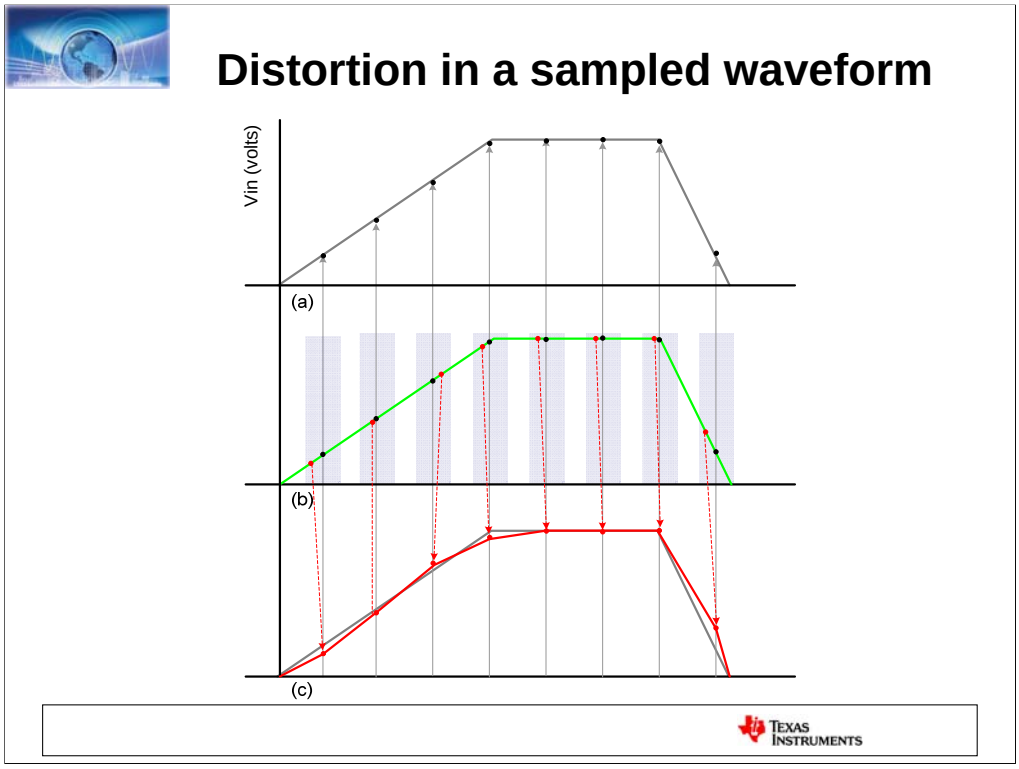
John D. Johnson
Manager
Strategic Marketing
Systems Engineering
Communications Clocking Group

214 567 2695
214 480 3555 Fax
214 502 3719 Cell
john-johnson@ti.com

Texas Instruments Incorporated
12500 TI Boulevard, MS 8701
Dallas, Texas 75243

Topics

- **Key ADC Parameters**
- **Phase Noise and Jitter**
- **Jitter Optimization**
- **Solution Examples**



Consider the three plots above.

The center plot represents a trapezoidal pulse (perhaps as captured on an oscilloscope). It is a continuous waveform (i.e. for each position in time on the horizontal axis there is a corresponding voltage on the horizontal axis).

The Black dots represent ideal sample points and these points are transposed to the plot on the top. The original waveform can be determined by connecting the points.

Superimposed over the center plot are regions which represent a possible location of a sampling point if there is jitter on the sample clock. While the top plot contains points which appear in the exact center of these regions, the actual sample point can appear randomly anywhere in the region. Some possible sample points are show as red dots on the center plot. These values are transposed to the plot on the bottom. Notice the value recorded is not the correct voltage level because it is sampled at the incorrect location. It is transposed to the point in time in which the sample was ideally to be taken (in the center of the sampling region). This results in the signal being distorted as shown by the red trace on the bottom plot.

Signal to Noise Ratio

Assuming a sinusoidal input for V_{in} we have,

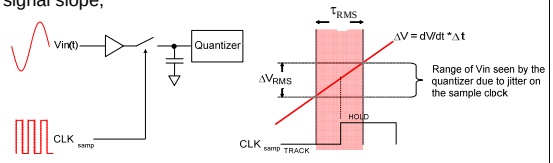
$v(t) = V_o \sin 2\pi ft$

Differentiating with respect to time yields the signal slope,

$$\frac{dv}{dt} = 2\pi f V_o \cos 2\pi ft$$

Taking the RMS value,

$$\frac{dv}{dt}_{rms} = \frac{2\pi f V_o}{\sqrt{2}} = \frac{\Delta V_{RMS}}{\tau_{RMS}}$$



Therefore, the RMS error voltage due to jitter is

$$\Delta V_{RMS} = \frac{2\pi f V_0 \tau_{RMS}}{\sqrt{2}}$$

Signal to noise ratio (SNR) is defined by,

$$SNR = 20\log_{10}\left[\frac{signal}{noise}\right] = 20\log_{10}\left[\frac{V_o/\sqrt{2}}{\Delta V_{rms}}\right]$$

Therefore, the SNR component due to jitter is:

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$

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The slide above shows the derivation of theoretical data converter SNR (Signal to Noise Ratio) due to jitter. It provides the following insight:

1. The frequency of the sample clock is not a factor.
2. The sample frequency of the data converter is not a direct factor, the input bandwidth of the data converter is (fmax).
3. The jitter value (tj) in Equation (6) represents total jitter which is the root sum squared of the sample clock jitter and the converter aperture jitter.

For many communications systems the bandwidth of the channel is fixed; however, the channel capacity needs to grow. Why?

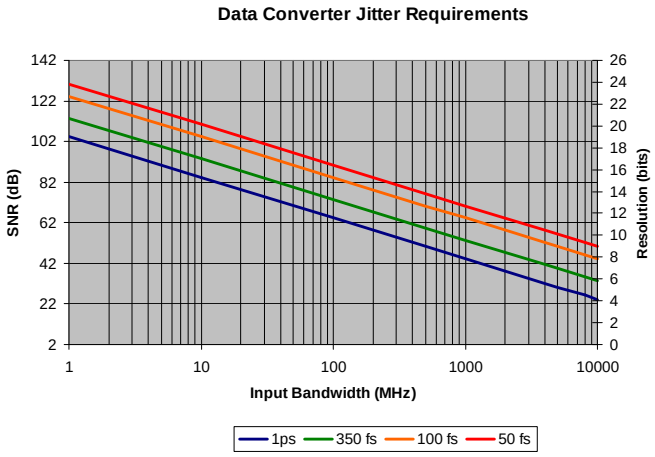
1. Multimedia content requires more capacity
2. High definition content requires more capacity
3. Growing populations and an expanding subscriber base requires more capacity.

In fixed bandwidth applications, SNR is the only lever engineers have to control channel capacity? What types of applications have fixed bandwidths?

Data Converter Clocking

$$SNR_{ADC} = 6.02N + 1.76$$

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$



- This figure plots SNR vs. input frequency for fixed values of jitter.
- We can note a couple of things about this graph
  - Lower jitter = better SNR
  - For a constant jitter, SNR decreases as the frequency of the sampled signal increases

Caveat emptor

Sampling jitter | Quantization Error | Input Noise

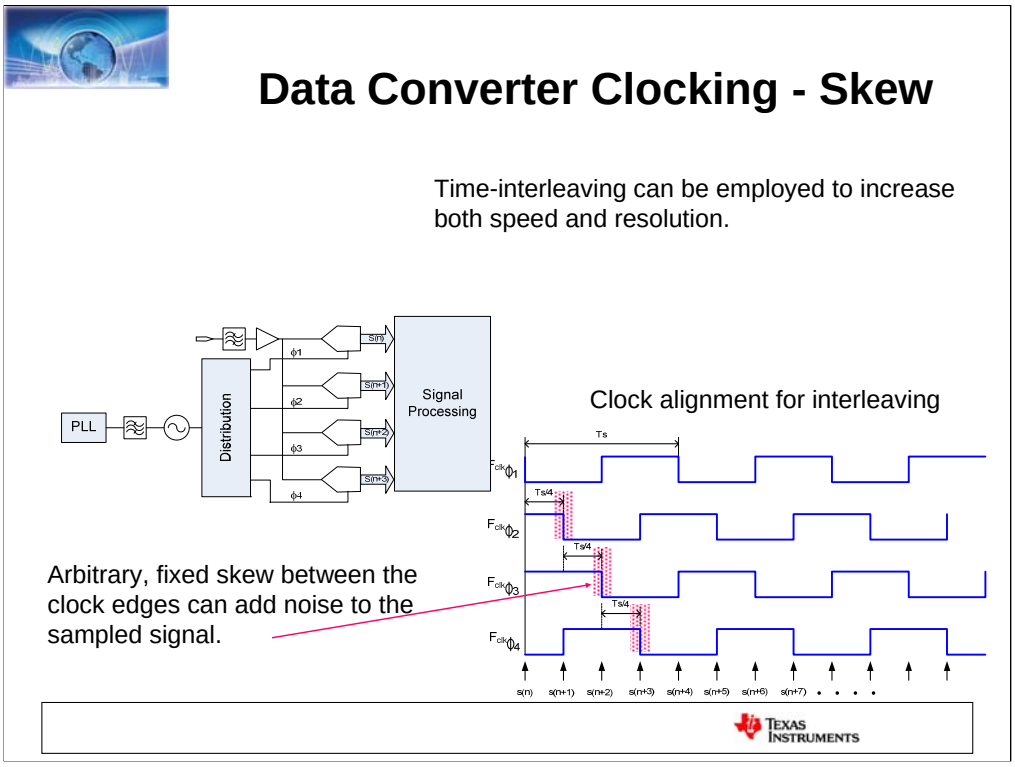
$$SNR = -20\log\left(\sqrt{\left(2\pi f_{in} t_{rms}\right)^2 + \frac{2}{3}\left(\frac{1+DNL}{2^N}\right)^2 + \left(\frac{2\sqrt{2}V_{noiserms}}{2^N}\right)^2}\right)$$

$$SNR_{ADC} = 6.02N + 1.76$$

(Full Scale Sine Wave with no clock jitter, DNL, or input referred noise)

Signal to Noise Ratio?

$$C = B \cdot \log_2(1 + SNR)$$



•Clock skew is a relative, *fixed* delay between two or more clock signals.

•It becomes relevant in systems that require fixed relationships between clocks.

- •Examples are designs that use multiple ADCs to capture data, or in synchronous data clocking.

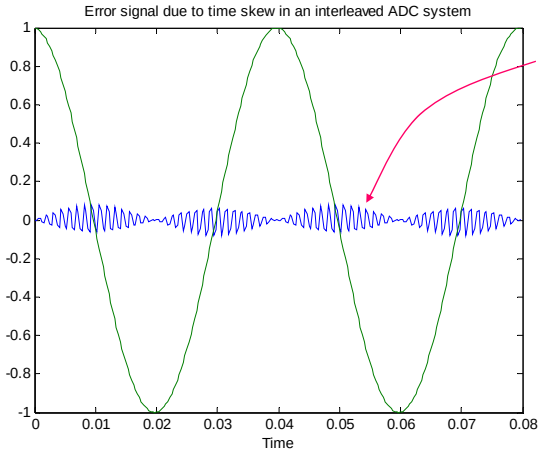
•The ADC applications tend to fall into two categories:

- •Interleaved ADC sampling for the purpose of achieving higher sample rates AND higher resolution (test and measurement, instrumentation)
- •Parallel multiple event capture (medical imaging, instrumentation, test & measurement)

•Interleaved sampling systems are used when off-the-shelf ADCs offer the required resolution but not the required sampling rate.

- •These systems use multiple ADCs clocked at the same rate. The effective increase in sample rate is achieved by a round-robin sampling scheme.
- •The timing diagram shows the ideal relationship between the clocks.
- •Each ADC runs at a rate of Fs. However, by staggering the clock phase between ADCs, the effective sampling rate becomes M * Fs, M= number of ADCs.
- •The ADC sample streams can be multiplexed into a single sample stream if needed

Error due to Skew in a waveform captured via interleaved sampling



Skew error =

ideal signal – signal with skew

This plot shows a sinusoid along with the error component due to skew.

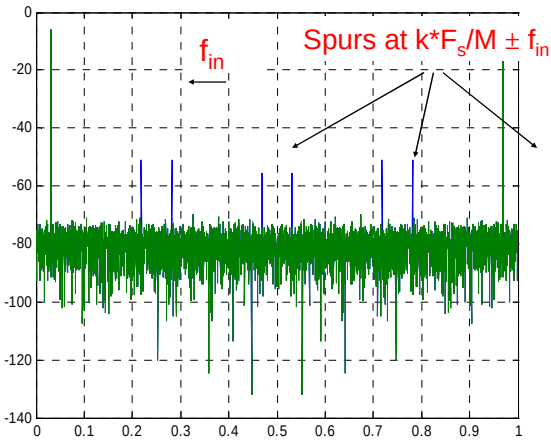
•If we could subtract the sampled signal with skew (green trace) from the ideal signal,

we would be left with the error signal (noise) due to clock skew, illustrated by the blue trace in the plot shown above.

•Note that the error reaches a maximum where the signal slope is maximum, and vice versa.

•How is this manifested in the frequency domain?

Skew in the frequency domain – interleaved sampled signal



F_s = sample frequency

M = # of ADC channels

k = 0,…,M-1

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- This plot shows that spurs are generated when clock skew is present.
  - The spur frequencies (blue traces) are determined by the frequency of the input signal and the number of ADC channels.
  - The spur amplitudes are determined by the frequency of the input signal and the relative values of the skew.

Summary

- Systems care about Signal to Noise Ratio for many reasons (e.g. Shannon's Equation).
- Signal to Noise Ratio is a parameter that can be optimized by:
  - Architectural Choices
  - Signal Chain Design
  - Component Choices
  - Careful Clock Design
- Clock Jitter and Skew are factors that directly influence ADC and hence overall signal chain performance.

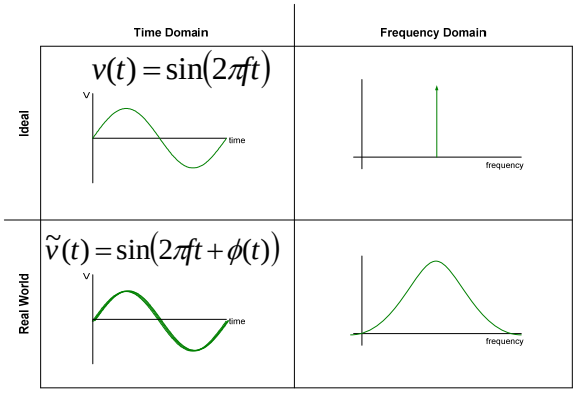
Topics

- Key ADC Parameters
- **Phase Noise and Jitter**
- Jitter Optimization
- Solution Examples

Why Consider Phase Noise?

- **Phase Noise and Jitter are directly related and we will need to understand this relationship, because:**
  - **Clock jitter directly impacts data converter performance, therefore in order to understand data converter clocking, we must first understand clock jitter and how to control it.**

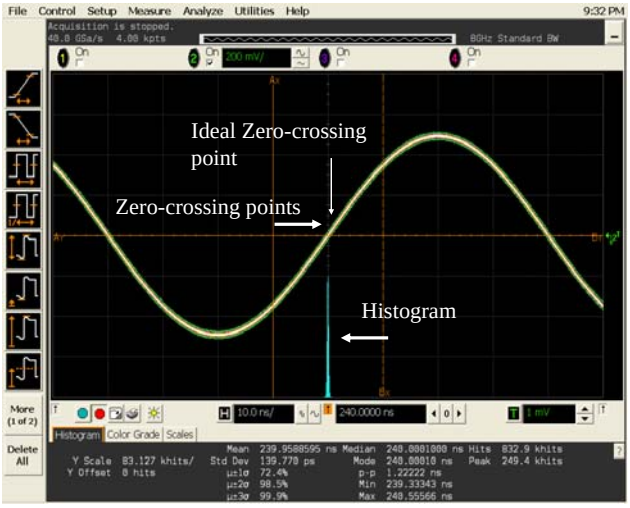
Phase Noise



Phase Noise Definition:

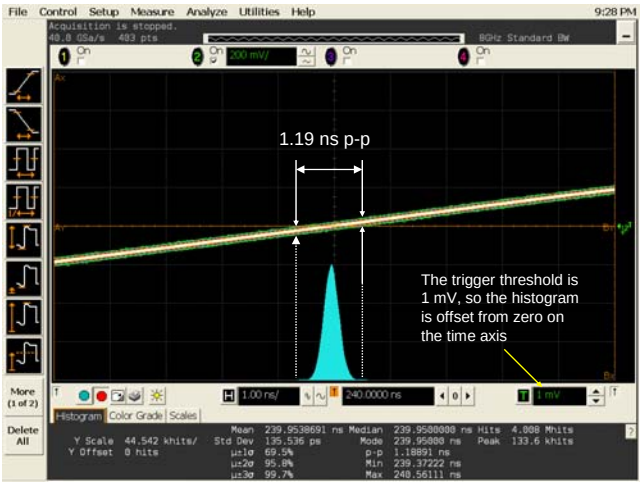
Rapid, short-term, random fluctuations in the phase of a waveform, caused by time domain instabilities.

Phase Noise in the time domain (1)



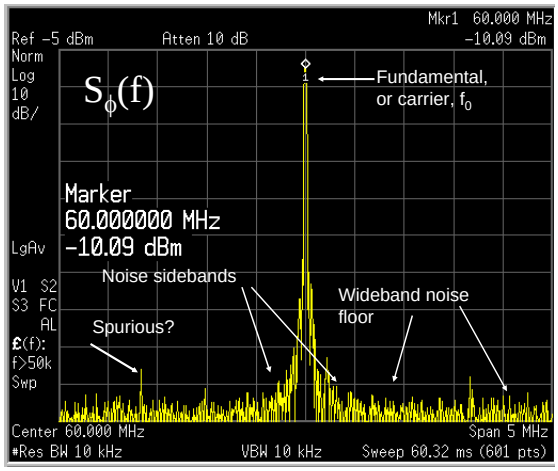
A digital scope is useful for viewing jitter in the time domain but is not adequate for measuring jitter due to limited time resolution

Phase noise in the time domain (2)



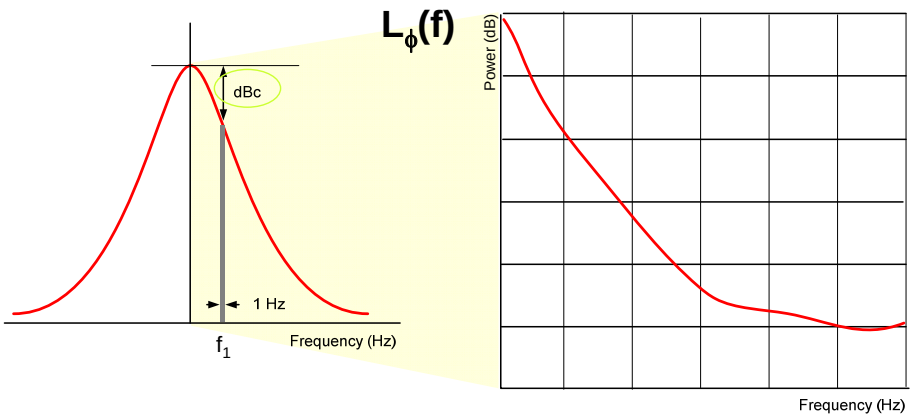
Expanding the time scale shows the Gaussian-like distribution of the jitter around the zero-crossing point

Phase Noise in the Frequency Domain



In the frequency domain, the noisy clock is not an ideal impulse. It appears as a spike with noise side bands that cause the base to spread.

Phase Noise Power Spectral Density (PSD)



Phase noise power is measured in a 1 Hz bandwidth at offsets from the carrier that cover a specified range of frequencies

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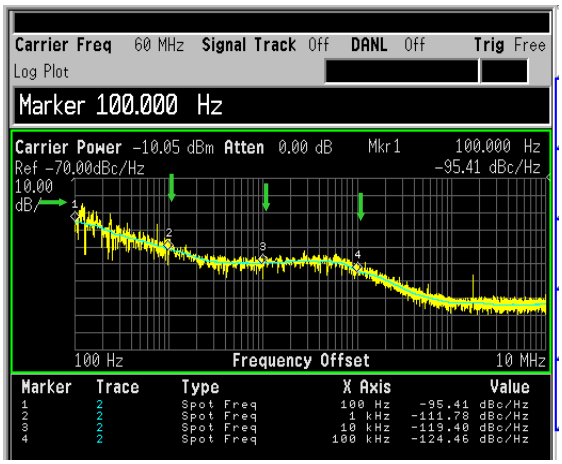
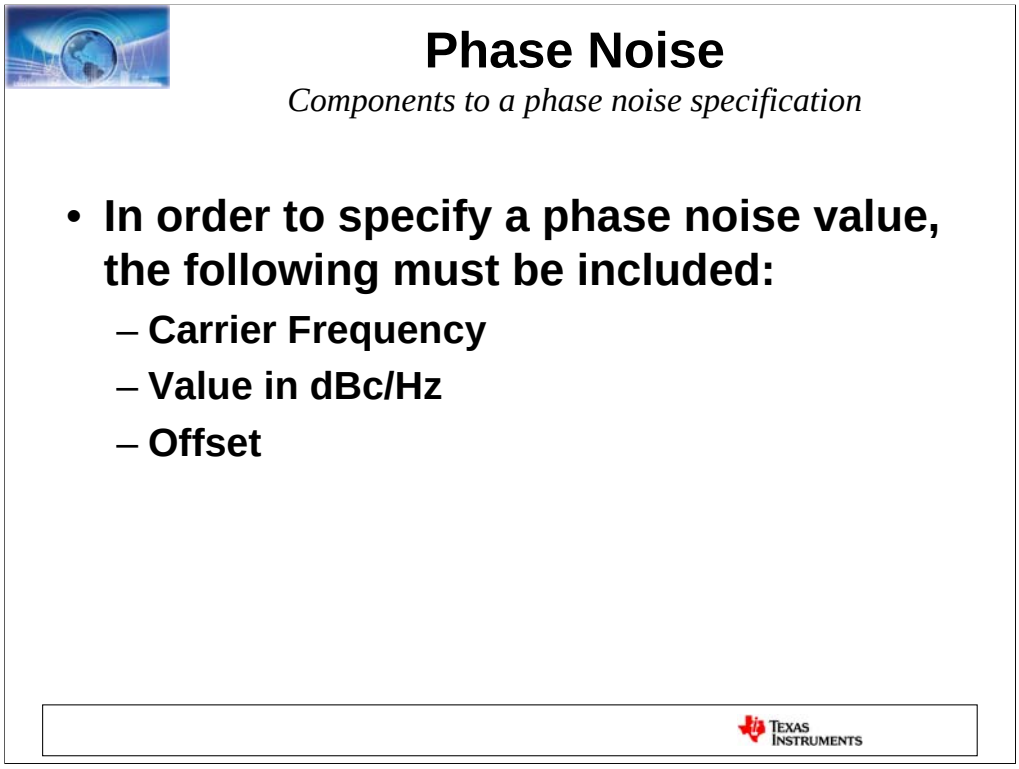
- Conventionally, the power spectral density (PSD) of the phase noise spectrum is specified in units of dBc/Hz.
- At a particular offset frequency (f_1), the spectrum analyzer measures the power in a 1 Hz bandwidth. Call this power P_{f1} Watts.
- To convert this to dBc, we take 10 times the log of the ratio of the carrier power (in Watts) to the phase noise power (in Watts):
  - $P_{dBc} = 10*\log(P_{carrier}/P_{f1})$
- By normalizing the phase noise power in this way, we can compare different oscillators without being concerned about the absolute power level of the oscillator.

Phase Noise: Frequency Domain



Specialized spectrum analyzers allows us to view and measure the phase noise PSD.



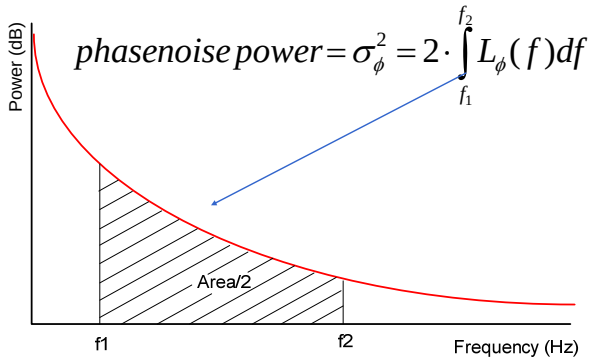
Phase Noise must be specified with these components:

1. The value: -93
2. The units: dBc/Hz
3. The offset from the carrier: 10 kHz
4. The carrier frequency: 1583 MHz

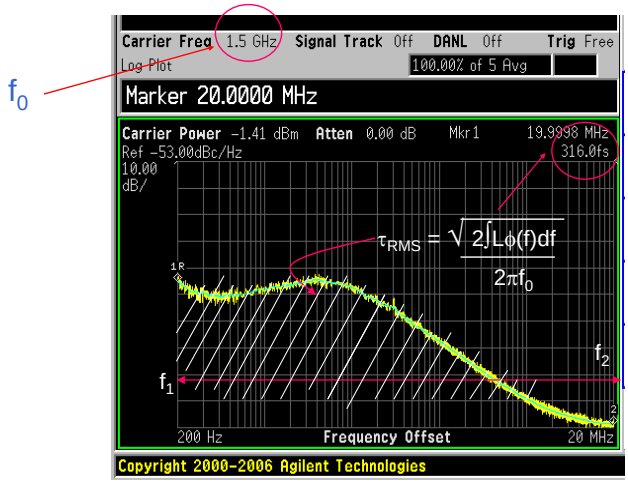
Integrated Phase Noise Power

$$power = \int_{-\infty}^{+\infty} S_{PSD}(f)df$$

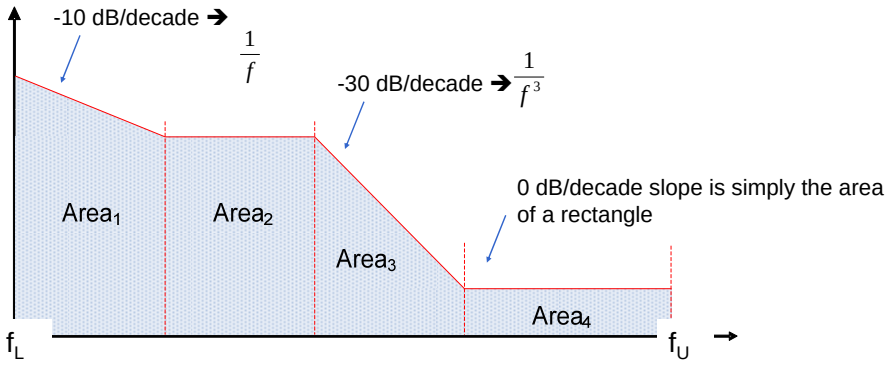
$$phasenoise\,power = \sigma_{\phi}^{2} = 2 \cdot \int_{f_1}^{f_2} L_{\phi}(f)df$$



Converting Phase Noise to RMS Jitter



Approximating the area under the curve



$$\int_{f_L}^{f_U} L_\phi(f)\,df \approx \sum_{\alpha} \text{Area}_1 + \text{Area}_2 + \text{Area}_3 + \text{Area}_4$$

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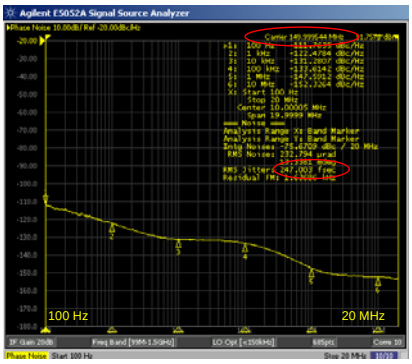
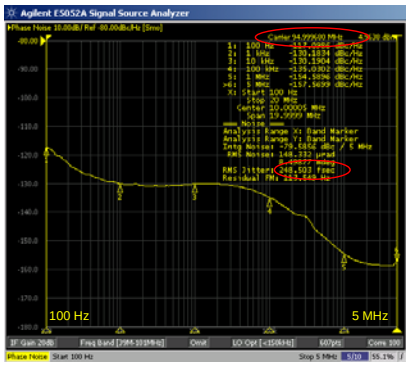
- This slide illustrates the area approximation method.
- Each slope of the log domain phase noise plot is converted to a straight-line approximation
- These straight line approximations will have the mathematical form: $-\alpha \log(f)$. For a slope of -10 dB/decade, $\alpha = 1$. Likewise, $\alpha = 2$ for a -20 dB/decade slope.
- In the linear domain, this is equivalent to a curve having the form $1/f^{\alpha}$ or $f^{-\alpha}$
- The noise sources found in PLLs and VCOs are often characterized in this way, using 1/f, $1/f^2$, $1/f^3$, etc. A well-known paper by Leeson describes this approach to modeling noise.
- Therefore, each sub-region under the curve is characterized by an equation of the form: $a_n*(1/f^{\alpha})$
- a_n is an appropriate gain term.
- The integral solutions for $1/f^{\alpha}$ are well known, so it is straightforward to integrate the area for each region, and then find the total area by summing the regions.
- This becomes the approximation for the total single sideband phase noise.

Comparing Clock Performance (1)

Can we compare these oscillators?

$$\tau_{RMS} = \frac{\sqrt{2 \cdot \int_{f_L}^{f_U} L_\phi(f)\,df}}{2\pi f_0}$$





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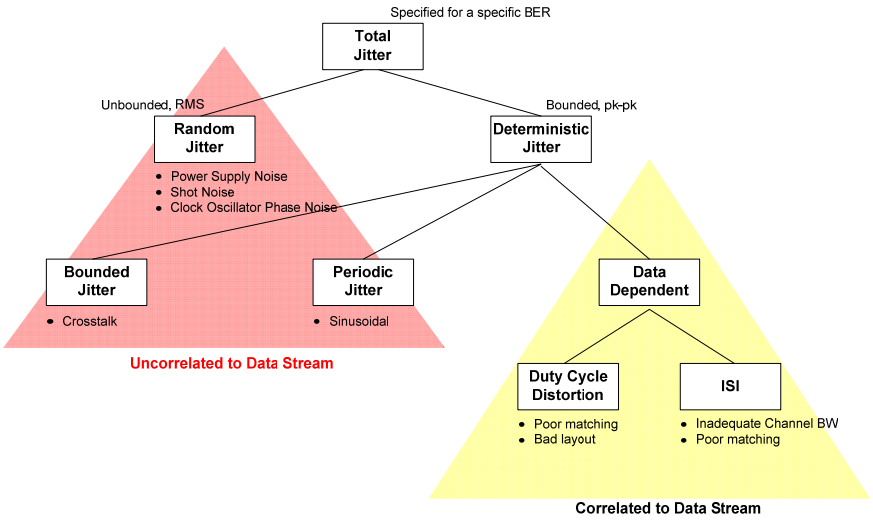
- When comparing RMS jitter or total phase noise between clocks, the ***limits of integration*** must be identical
  - Comparing two clocks that have different phase noise bandwidths is invalid
- When comparing RMS jitter between clocks, ***the carrier frequencies*** must be identical
  - Remember, jitter is proportional to the inverse of the clock frequency.
  - If two clocks have the same phase noise power but operate at different frequencies, the clock at the higher frequency will have lower jitter.
- Total (integrated) phase noise power says nothing about the distribution of the noise.
  - PSDs having different shapes may yield the same total phase noise power
- A good clock can be made to look bad if a wider region of integration is chosen relative to a lower quality oscillator

Comparing Clock Performance (2)

- **It is possible to re-normalize phase noise data for clocks of different frequencies in order to compare them.**

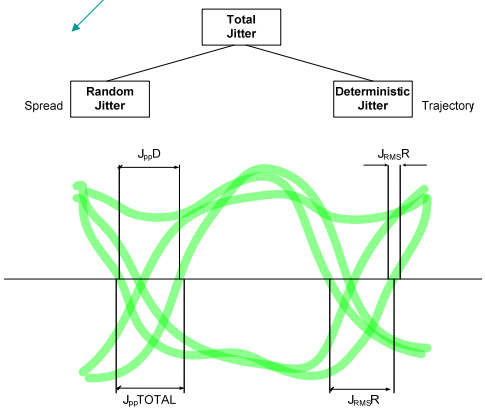
$$S_{new}(f)_{dB} = S_{old}(f)_{dB} + 20 \cdot \log_{10}\left(\frac{f_{new}}{f_{old}}\right)$$

Jitter Tree


Specified for a specific BER
Total Jitter
Unbounded, RMS
Bounded, pk-pk
Random Jitter
Deterministic Jitter
Power Supply Noise
Shot Noise
Clock Oscillator Phase Noise
Bounded Jitter
Periodic Jitter
Data Dependent
Crosstalk
Sinusoidal
Uncorrelated to Data Stream
Duty Cycle Distortion
ISI
Poor matching
Bad layout
Inadequate Channel BW
Poor matching
Correlated to Data Stream

Elements of Total Jitter

The dominant noise component of a clock signal is Random Jitter.



Random Jitter (RMS jitter) is derived from the phase noise plot of the clock signal.

Phase Noise Summary

- Phase noise is the instantaneous, random deviation in the ideal phase of a clock signal.
- Phase noise is observed in the frequency domain using a spectrum analyzer to plot the power spectral density of the phase noise.
- Total power of the phase noise in a specific frequency band is found by summing the area under the phase noise density curve for that band.
- RMS jitter is derived from RMS phase noise by normalizing the phase noise to the carrier frequency.
  - RMS jitter represents the area under the PSD curve
  - Integration limits must be included when specifying RMS jitter

Topics

- Key ADC Parameters
- Phase Noise and Jitter
- **Jitter Optimization**
- Solution Examples

Phase Noise Optimization Introduction

- We have learned that Phase Noise is related to Jitter.
- We have learned that Clock Jitter degrades the Signal to Noise Ratio (SNR) performance of a data converter.
- Now we will study how to optimize (minimize) clock phase noise and hence clock jitter.

PLL – 'The Impersonator'

Desired: Signal with wide tuning range, good accuracy and stability, and acceptable phase noise.

	Oscillator 1: Crystal Reference	Oscillator 2: VCO	PLL Output
Tuning Range (pulling)	**Narrow**	Wide →	Wide
Accuracy	Very Good	**Poor** →	Very Good
Phase Noise	Superb: close in **Poor: far out**	**Poor: close in** Very Good: far out →	Good: close in Very Good: far out
Stability and Drift	Potentially Good	**Poor** →	Good

A PLL can substitute **desirable performance characteristics** for **undesirable characteristics**.

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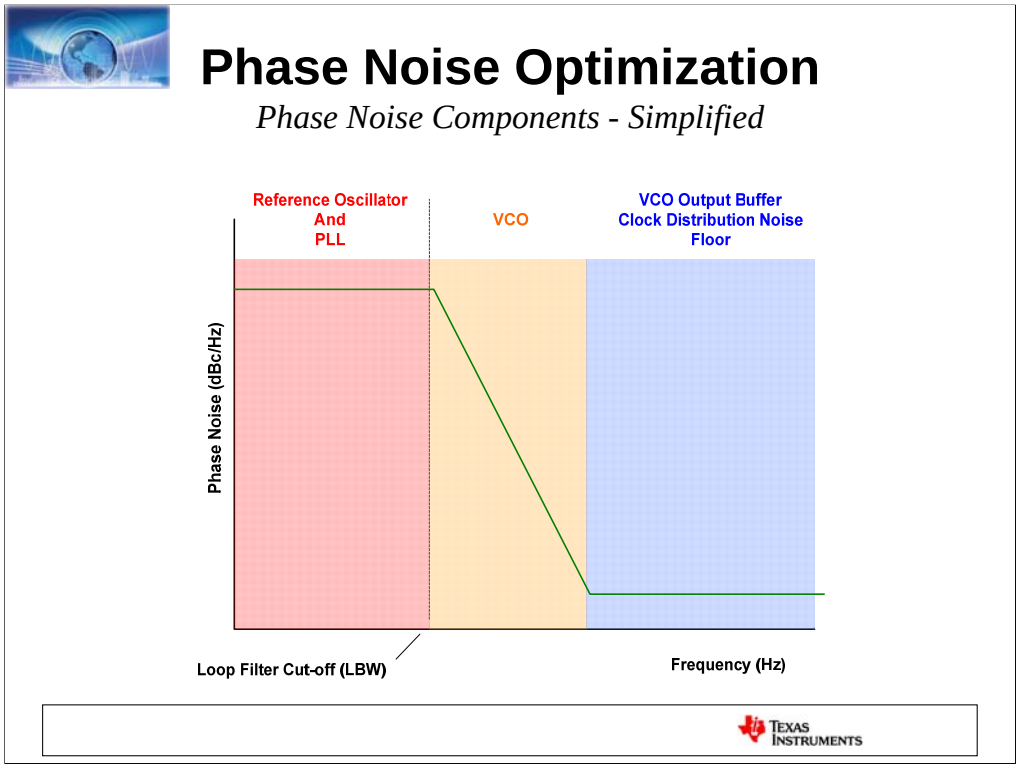

•The diagram above shows three primary regions in the frequency domain, in terms of offset from the carrier frequency of the clock.

•In each region, certain functions or components in the PLL will be the major noise sources

Close into the carrier, the noise of the reference oscillator dominates. Moving slightly away from the carrier, the noise of the PLL takes over. The point at which the VCO becomes a factor is determined by the bandwidth of the loop filter.

For the most part, the primary lever that a designer has to control the shape of the phase noise profile is the loop filter of the phase locked loop.

Let's look at some specific examples courtesy of EasyPLL.

Phase Noise Optimization - Levers

PLL Functional Block	To minimize Noise contribution…	Why?
Phase Detector/Charge Pump	**Maximize charge pump gain (K_ϕ) (up to a certain point)**	**The phase detector noise contribution is proportional to $1/(K_\phi)^2$**
R-counter and N-counter divide ratios	**Maximize phase detector compare frequency → this minimizes N**	**The noise contribution of the R and N dividers is proportional to N^2.**
Reference oscillator	**Use highest frequency practical and use R > 1 if possible. If deciding between maximizing R and minimizing N, minimize N.**	**The noise contribution from the reference oscillator is proportional to $(N/R)^2$**

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•This table provides some guidance on design choices in PLL/VCO design that can be manipulated to improve phase noise performance.

•Keep in mind that no amount of clever design or optimization can overcome the use of poor quality components

•Using the best reference clock and VCO that meet cost targets is always a given.

•If close-in phase noise is important for a particular application, then choose components that give the desired close-in performance and acceptable performance at higher offsets.

Selecting Loop BW

Condition	Loop Bandwidth	Why?
Noisy reference input. **Good VCO.**	**A narrow loop bandwidth would be used to minimize the contribution of the reference input.**	**A narrow bandwidth allows the VCO performance to dominate. This why a high quality VCO is normally used.**
Good reference. **Noisy VCO**	**A wide loop bandwidth would be used to allow the reference to dominate inside the loop bandwidth**	**This will minimize the overall noise profile and total noise power because the VCO noise is suppressed inside the loop.**

PLL Summary

- PLL parameters such as R, N, K_ϕ, K_{VCO} and the loop filter bandwidth will influence the overall noise performance at the output.
- Each function in a PLL/VCO clock circuit contributes to the overall noise at the output of the VCO
- The loop transfer function for each noise source determines the frequency region of the phase noise in which the respective noise source will dominate in final output.

Topics

- Key ADC Parameters
- Phase Noise and Jitter
- Jitter Optimization
- **Solution Examples**

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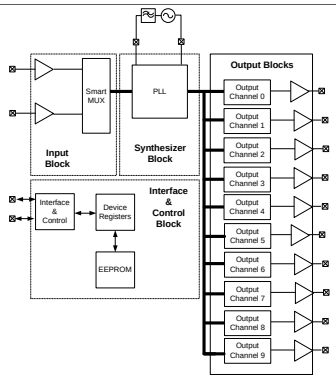
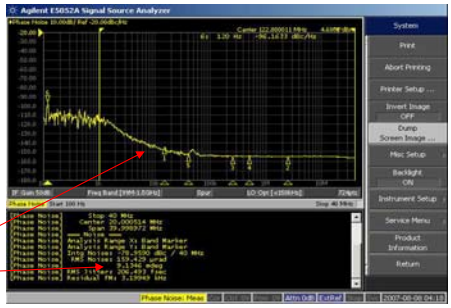


- Clock Generator, Jitter Cleaner Modes
- < 50 fs Residual Jitter
  - 200 fs RMS Jitter with good VCO
- Two Universal Inputs
  - Differential or Single Ended
- Smart Multiplexer
  - Automatically switches between inputs
- On board PLL
  - External VCO/VCXO and loop filter
  - Holdover Mode Supported
- 10/20 Outputs (10 differential, 20 single-ended)
  - Programmable (LVDS, LVPECL,LVCMOS)
  - Adjustable Skew
  - Dedicated Divide Ratio per Channel
- On-chip EEPROM determines default state at power up
- Fully programmable via SPI port.



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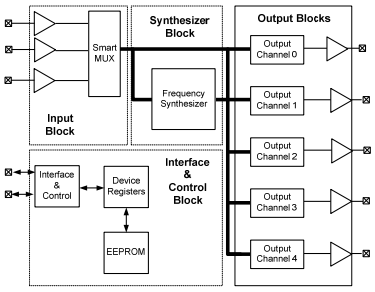
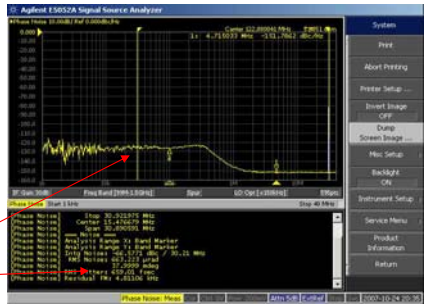


- Clock Generator, Jitter Cleaner, and Fan-out Buffer Operational Modes
- < 1 ps RMS Jitter
- Two Universal Inputs (up to 1500 MHz)
  - Differential or Single Ended
- One Crystal Input
  - Oscillator Port supports Holdover and SERDES startup modes.
- Smart Multiplexer
  - Automatically switches between inputs
- On board synthesizer including PLL, VCO, and loop filter
- 5/10 Outputs (5 differential, 10 single-ended)
  - Programmable (LVDS, LVPECL,LVCMOS)
  - Adjustable Skew
  - Dedicated Divide Ratio per Channel
- On-chip EEPROM determines default state at power up
- Fully programmable via SPI port.



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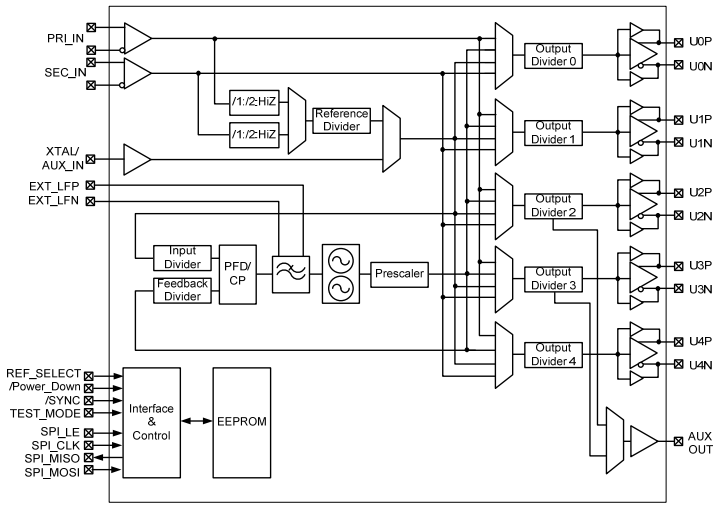
September Production



FFT Refresher

- Fs = Sampling Rate = 80MS/s
- Fin = Input Frequency = 70MHz
- N = Number of Points
- Fbin = FFT Bin Width

$$Fbin = Fs / N$$

N = 32K and Fs = 80MS/s	Fbin = 2441Hz
N = 256K and Fs = 80MS/s	Fbin = 305 Hz
N = 512K and Fs = 80MS/s	Fbin = 153 Hz

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FFT Refresher

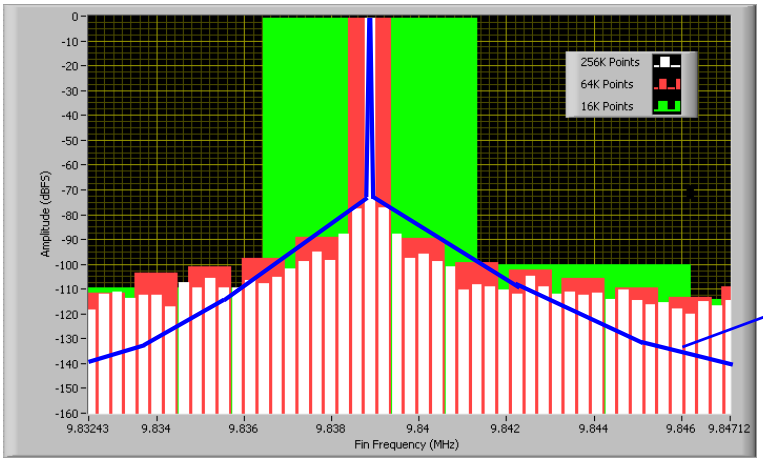
- **Fs = Sampling Rate = 80MS/s**
- **N = Number of Points**
- **SNR = ADC noise**
- **Noise_Floor = Average Noise from SNR**

$$Noise\_Floor = 10 \bullet LOG\left[\frac{10^{-SNR/10}}{N/2}\right]$$

N = 32K and SNR = 75dBFS Noise_Floor = -117dBFS
N = 256K and SNR = 75dBFS Noise_Floor = -126dBFS
N = 512K and SNR = 75dBFS Noise_Floor = -129dBFS

The Problem – FFT Performance

Real ADS5433 at 80MS/s and 70MHz (Using 8644Bs)



Clock Phase Noise

Clock Jitter Considerations in the Lab

- **Minimum number of points (N) for DC performance is 4 x 2^M, where M is the ADC bit resolution (to ensure no missing codes for INL, DNL of ADC)**
- **Number of points (N) for optimal AC performance (SNR) is about 2^{M-1} to 2^M, where M is the ADC bit resolution**
- **Any variation in clock jitter within Fbin (Fs +/- Fbin/2) is not important**
- **For Nyquist system, wideband phase noise up to Fs/2 is important**
- **Clock phase noise in wide band aliases back into close-in phase noise**

$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$

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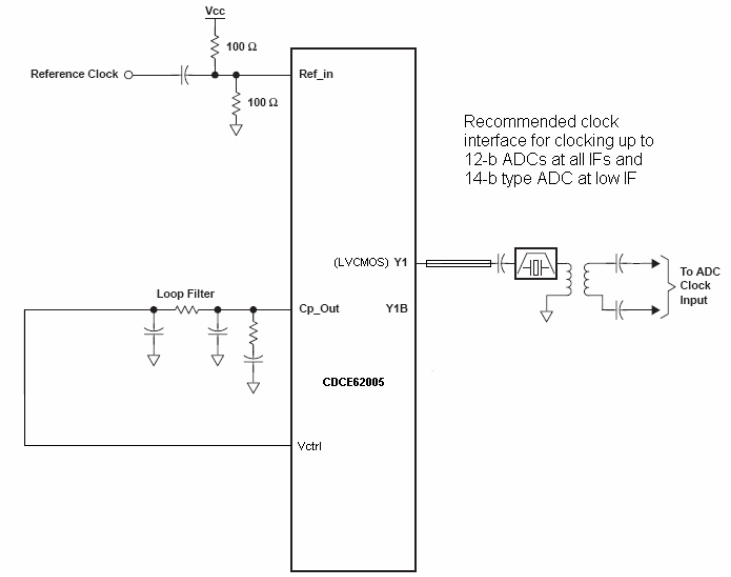
Clock Jitter Considerations in the Application

- Close-in and far-out phase noise important for all applications
  - Clock phase noise in wide band aliases back into close-in phase noise
- Start & stop bandwidth for clock jitter dictated by any conforming industry standard or customer/application requirement
- For example, in wireless BTS systems
  - Clock integration bandwidth would depend on channel spacing and channel bandwidth

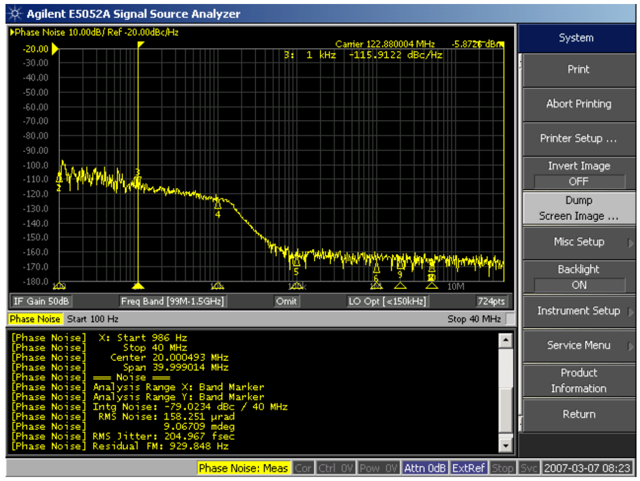
$$SNR_{jitter} = 20\log_{10}\left[\frac{1}{2\pi f_{\max}\tau_{RMS}}\right]$$

Clock Interface to ADC



Clock Interface to ADC

CDCE72010/CDCM7005 LVPECL (CDCE62005 + BPF)



TEXAS INSTRUMENTS

Clocking ADCs

CDCE72010/CDCM7005

Advantage: Very low output jitter, very high jitter cleaning ability, great for clocking high bit resolution high IF ADCs and all DACs
Disadvantage: Cost, Board space (large external components)

CDCE62005

Advantage: Low output jitter, good jitter cleaning ability, good level of integration, great for clocking up to 12-b ADCs for mid-IFs and all DACs, no need for VCXO
Disadvantage: On-chip VCO has lower Q, can't be used to clock >12-b ADCs

ADS5525

12-bit, 170MSPS ADC with CMOS & DDR LVDS Outputs

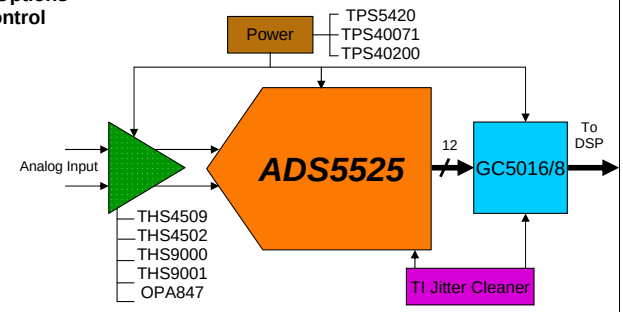
Features

- Maximum Sample Rate: 170 MSPS
- 12-Bit Resolution; No Missing Codes
- Power Dissipation: Core 1 W, Total 1.13 W
- 11 ENOB Guaranteed at 70-MHz IF
- Programmable power scaling
- 70.5-dBFS SNR at 70-MHz IF
- 84-dBc SFDR at 70-MHz IF
- Internal Sample and Hold
- Parallel CMOS and DDR LVDS Output Options
- Selectable Output Timing and Level Control
- Internal or External Reference
- 3.3-V Analog and Digital Supply
- 48-Pin QFN Package (7 mm x 7 mm)

Applications

Benefits

- Highest SNR and SFDR available 12-bit 170 MSPS sample rate
- Space saving QFN package – smallest package available
- Increased performance benefits a variety of test and measurement, communications and imaging applications.



EVM

ADS5525EVM
Samples and EVMs available

Texas Instruments

ADS5525 Clocking

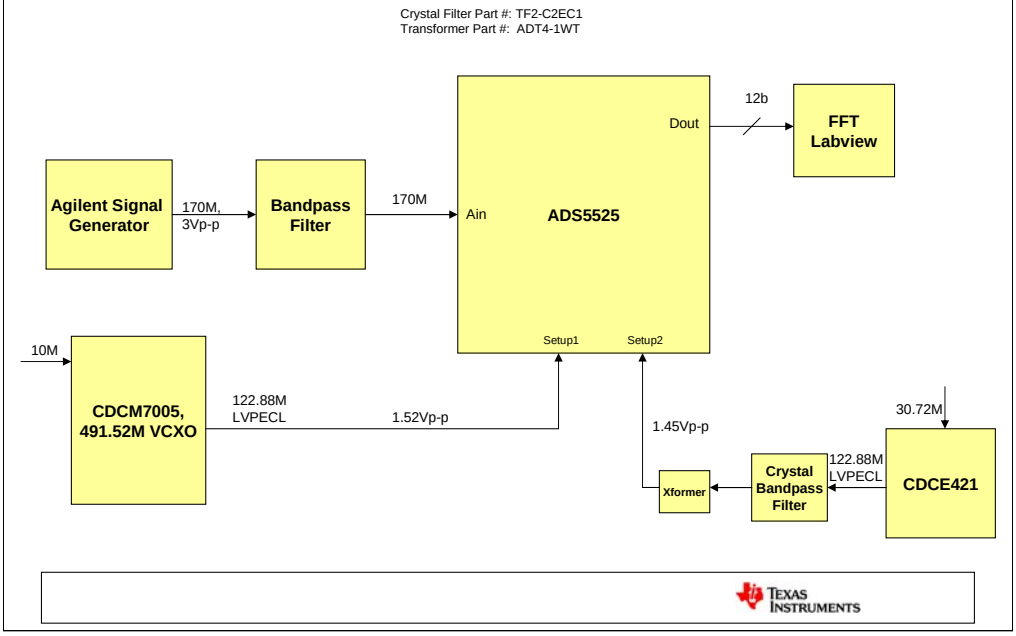
Calculate Required Clock Jitter to achieve desired SNR

Input Frequency	**170.00**	**MHz**	**desired input frequency to ADC analog inputs**
Aperture Jitter	**150.00**	**fs rms**	**aperture jitter comes from ADC datasheet**
Ext Clock Jitter	267.25	fs rms	**rms jitter of clock source at ADC clock inputs**
Total Jitter	**306.47**	**fs rms**	**rms jitter of clock and ADC jitter combined**
SNR	**69.70**	**dBc**	**Signal-to-Noise Ratio of ADC**

Datasheet performance

http://www.ti.com/litv/zip/slac133

Test Setup

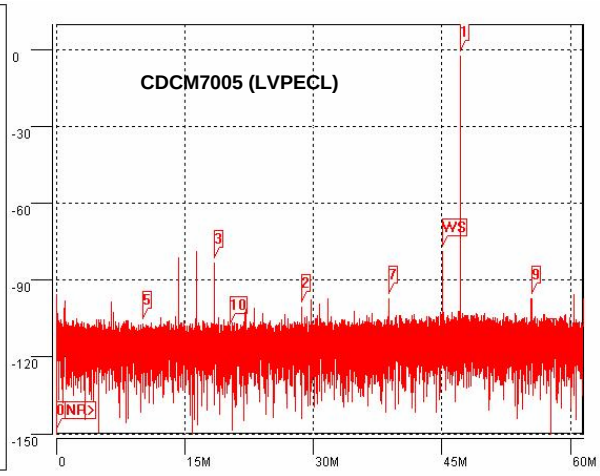

Crystal Filter Part #: TF2-C2EC1
Transformer Part #: ADT4-1WT
Agilent Signal Generator
170M, 3Vp-p
Bandpass Filter
170M
Ain
ADS5525
Dout
12b
FFT Labview
Setup1
Setup2
10M
CDCM7005, 491.52M VCXO
122.88M LVPECL
1.52Vp-p
1.45Vp-p
30.72M
Xformer
Crystal Bandpass Filter
122.88M LVPECL
CDCE421
Texas Instruments

ADS5525 Performance

Device	IF (MHz)	Clock (MHz)	SNR (dB)	SFDR (dB)	D/S SNR (dB)	D/S SFDR (dB)
CDCE421 + BPF (CDCE62005 + BPF)	**170**	**122.88**	**69.63**	**78.59**	**69.7**	**79**
CDCM7005/LVPECL	**170**	**122.88**	**69.66**	**78.42**	**69.7**	**79**

ADS5525 FFT

Fin : 170.00 Mhz
Fs : 122.88 Mhz
Fund Ampl : -2.31dB
SFDR : 78.42dB
THD : -80.47dB
SNR : 69.66dBFS
SINAD : 68.57dBFS
HD2 : -98.26dB
HD3 : -80.96dB
ENOB : 11.15 bits



ADS62P15

Dual channel 11 Bit 125 MSPS ADC with "*SNRBoost*"

Features

- **11-bit resolution with No Missing Codes**
- **66.0 dBFS SNR at 70 MHz IF**
- **76.0 dBFS SNR at 70 MHz IF, 20 MHz BW using TI proprietary *SNRBoost* technology**
- **83 dBc SFDR at 70 MHz IF**
- **3.5dB Coarse Gain and Programmable Fine Gain up to 6dB for SNR/SFDR trade-off**
- **Parallel CMOS and DDR LVDS Output Options**
- **790 mW Total Power Dissipation**
- **64-QFN Package (9mm x 9mm)**

Applications

- Communications IF Processing & Basestations
- Test Equipment
- Medical Imaging
- Video and CCD Digitizing

Benefits

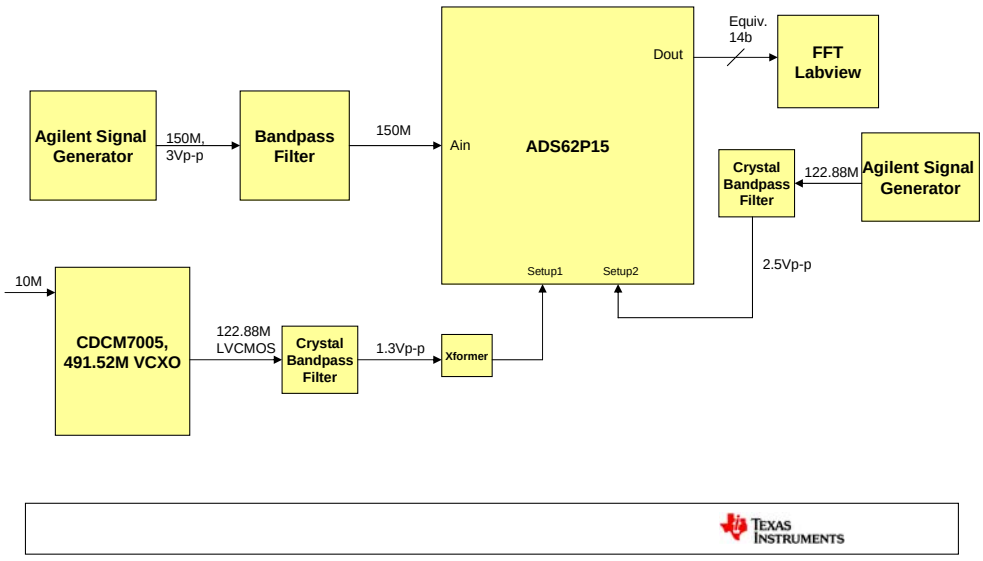
- Equivalent 14bit in-band SNR performance and superior SFDR performance enables higher sensitivity
- SNR/SFDR trade offs provide optimization of design performance under different requriement
- Lower power consumption eases heat management
- Small package reduces board space and improves signal integrity

Bandwidth	Default Mode	With *SNRBoost*
5 MHz	77 dB	81.5 dB
10 MHz	74 dB	79.7 dB
15 MHz	72 dB	77.0 dB
20 MHz	70 dB	76.0 dB

Texas Instruments

Test Setup

Crystal Filter Part #: TF2-C2EC1
Transformer Part #: ADT4-1WT



ADS62P15 Performance

Device	IF (MHz)	Clock (MHz)	SNR (dB)	SFDR (dB)
Agilent Signal Generator	**150**	**122.88**	**76.32**	**87.21**
CDCM7005/LVCMOS + BPF	**150**	**122.88**	**78.1**	**97.5**

ADS62P15 FFT

CDCE72010/CDCM7005 LVCMOS + BPF