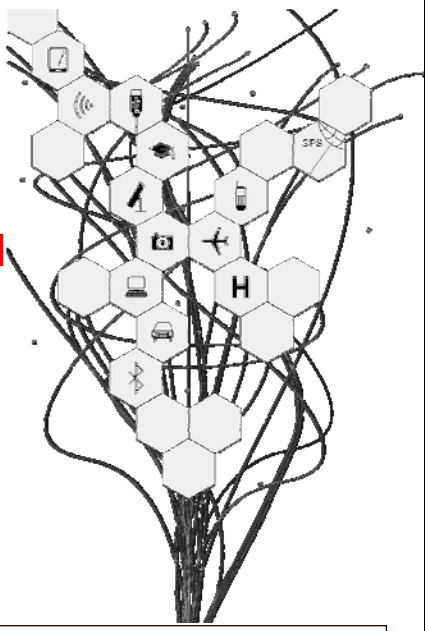
OMAP35x Processors Inspire New Applications with Unprecedented Performance at Handheld Power Levels

July 2008



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•OMAP35x processors is TI's first generally available, HIGH performance ARM solution. It will give you extremely high performance capabilities, similar to those you might find in some laptops, at power levels similar to what you would find in a cell phone.

Agenda

- Catalog Processors Introduction
- OMAP35x Silicon Platform
- OMAP35x EVM Tools and Software
- OMAP35x and Open Source
- OMAP35x Power and Analog Solutions

Blue underlined text indicates hyperlinks


Indicates portion of the slide are “clickable” for more information


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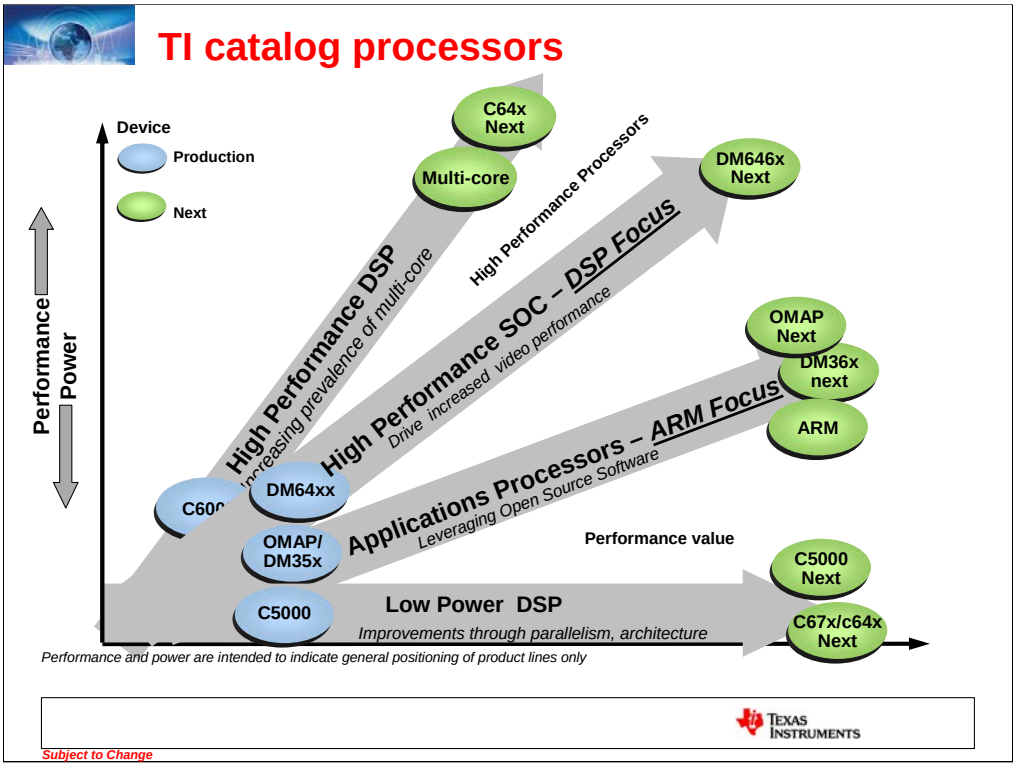


•Catalog processors is organized based on four distinct vectors

•Low power DSP

- •Currently utilizing our c5000 family
- •Focused on improving and reducing power consumption through architecture advancements and parallelism

•Applications processors

- •Predominantly focused on ARM / general purpose processing either for very high performance or value solutions
- •Heavily leverage open source activities and initiatives relating to general purpose processors
- •May or may not contain DSP's or DSP technology

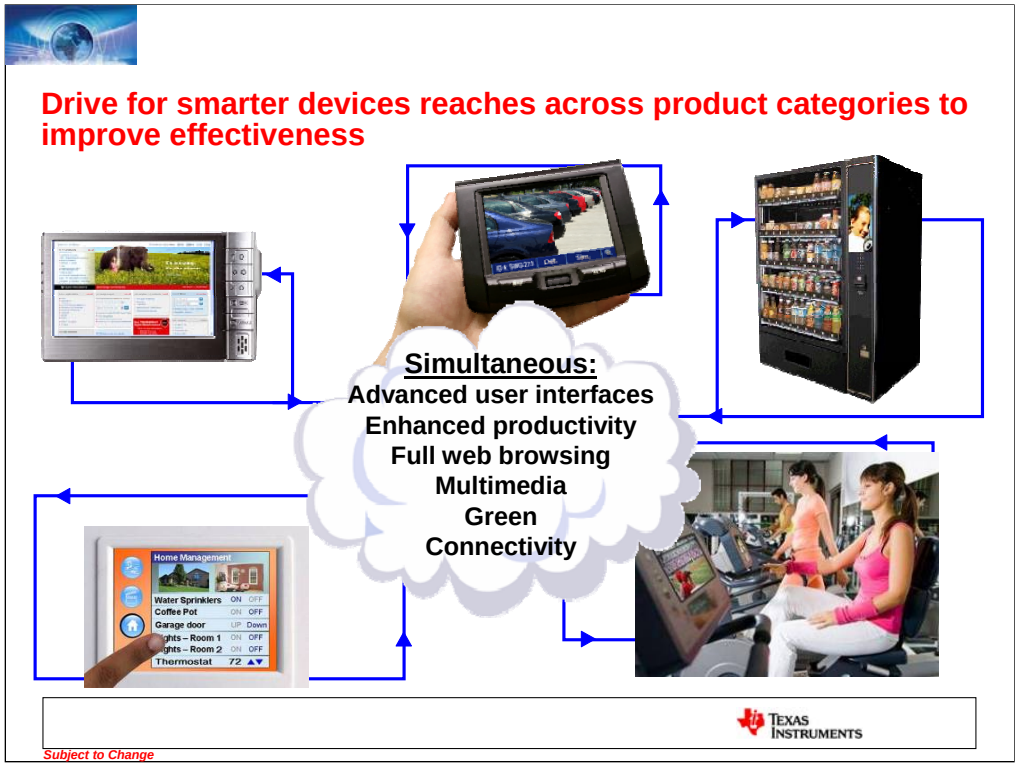
•High Performance SOC

- •Largely focused on absolute highest performance across all cores ARM + DSP or ARM + accelerators.
- •May or may not contain ARM / general purpose processors

•High performance DSP

- •Very focused on incredibly computationally intensive tasks
- •Almost 100% DSP based utilizing multiple DSP cores

OMAP35x silicon platform



•There are two main vectors inherent in most advanced electronics markets today.

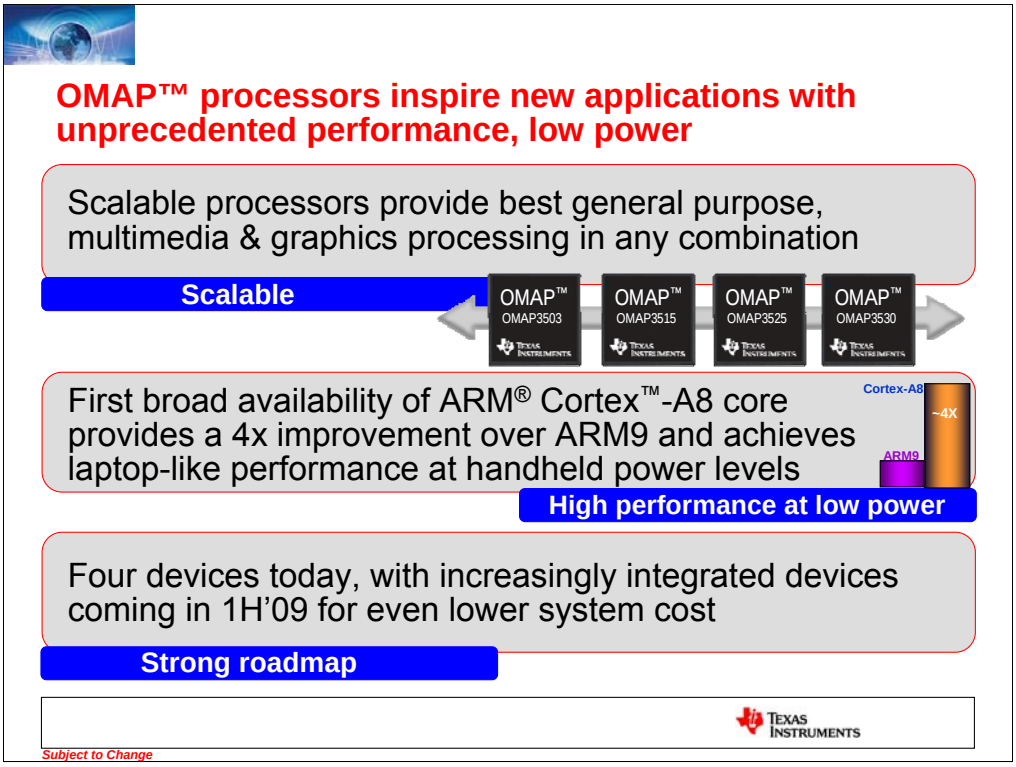
•The first vector is a trend of always connected whether it is to the Internet, corporate network, industrial software, or simply the next device.

- •This vectors drives the need to present enormous amounts of information to the user.

•The second vector is one of low power. In many cases this will apply not only to battery powered or portable devices where OEM's, ODM's, and manufactures need days of battery life, but also to line powered devices where companies are being driven to be more ecologically friendly or "green".

•These two, intuitively divergent, vectors present a unique challenge to equipments makers. Manufactures have to make a product that is incredibly simple to use, one that cannot need an instructions book. This same product has to be inviting to the user such that they will want to interact with it. Furthermore in many cases this has to be done on increasingly smaller form factors to reduce weight and ultimately cost.

•This is where OMAP excels and exactly why we are making it available to the broad market



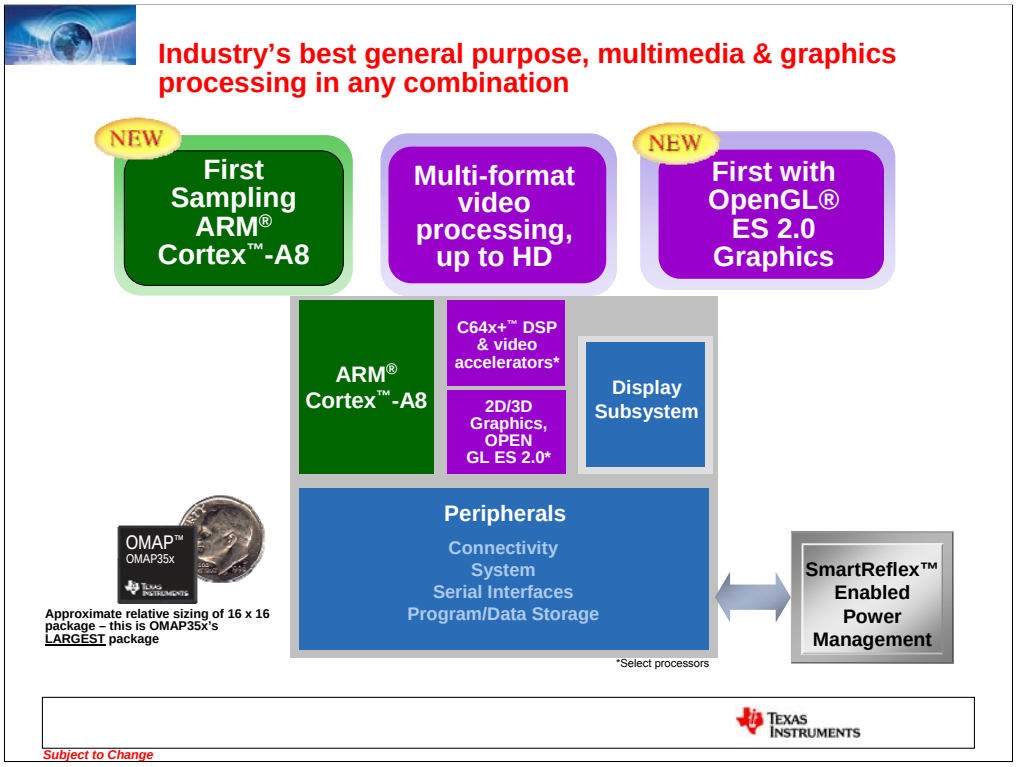
•The OMAP35x platform consists of four devices, the OMAP3503, 3515, 3525, and 3530. Among these four device TI offers very powerful combination of general purpose processing, multimedia, and graphics, in any combination. This overall platform allows scaling to meet just the needs of the product being designed.

•TI has historically been a leader in shipping ARM based solutions to the market. Keeping with this tradition, this is the first broadly available ARM Cortex A8 offering. The Cortex A8 offers approximately a 4x boost in performance when compared to a 300 MHz ARM 9. 2x is achieved based on increased clock speed and 2x is achieved based on an increase in mips per mhz efficiency.

•When compared to an ARM11 CortexA8 is approximately 2x the efficiency plus any clock speed increase there is.

•While these four devices are extremely competitive, they are just the beginning. Our roadmap devices are already in the works for release in 1H'09 and include things like emac, 3.3V IO and more.

•Samples of the OMAP35x are available today as well as the OMAP35x EVM.



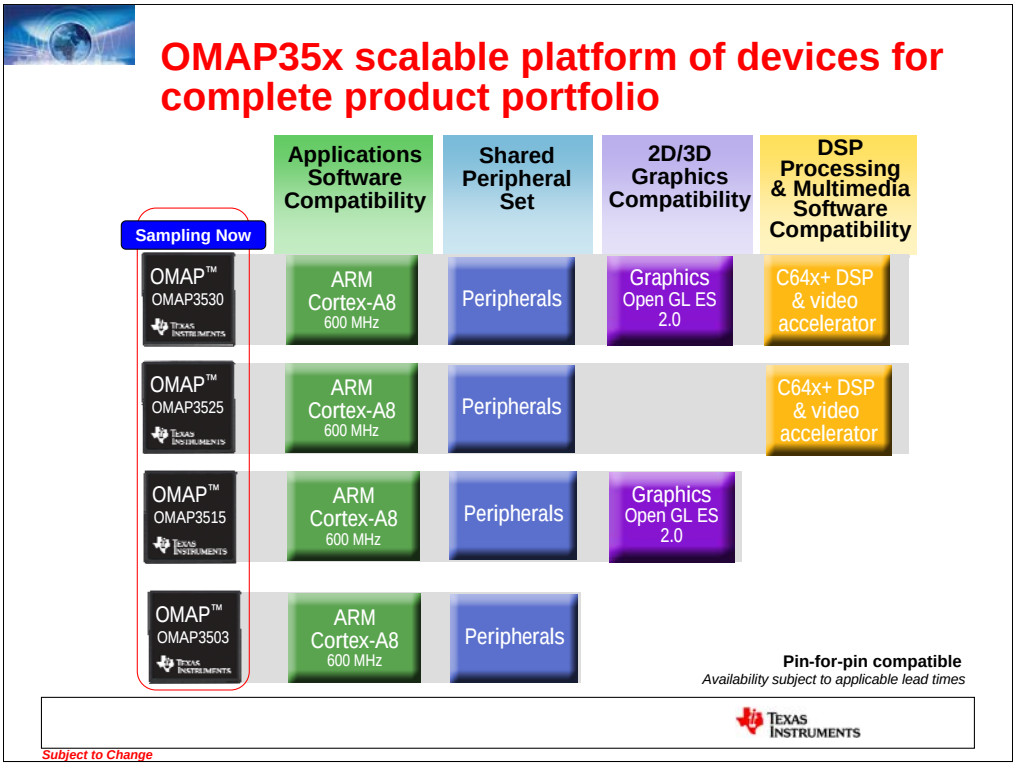
•OMAP35x brings together the capability to have very high performance general purpose processing, video / multimedia processing, graphics acceleration, and a highly integrated peripheral set all in one very small package.

•The launch of the OMAP35x marks the first general availability of the Cortex A8 core to the mass market. This core offers an enormous lift over ARM9 and ARM11 cores.

•Enabled along side this core is DSP + accelerator engine capable of offering up to 720p HD video processing.

•This release of PowerVR SGX graphics accelerator marks the first time a integrated, embedded solution has had OpenGLES2.0 compatibility included in hardware.

•All of this combined with TI's Smartreflex power saving technology provide an optimal blend of performance, power, and integration.



•The OMAP35x platform currently consists of four devices.

•The initially available devices is the OMAP3503 which consists of dual issue, superscaler ARM Cortex A8 plus a highly integrated peripheral set.

•The next device in the platform is the OMAP3515 which keeps the same ARM and peripherals and add in an Open GLES2.0 compatible graphics engine

•The third device in the offering is the OMAP3525 which removes the graphics engine and adds TI's c64x+ DSP and proprietary video accelerators

•The flagship device is the OMAP3530 which integrates all the components shown

•Most importantly all device are pin-to-pin compatible for easy vertical scalability

•All devices are sampling today

OMAP35x processor Laptop like performance at handheld power level

Performance

- High-performance Superscalar ARM® Cortex™-A8 featuring NEON co-processor with immersive 2D/3D Graphics accelerator
- HD video decode utilizing TMS320C64x+ DSP and video hardware accelerators
- Low power utilizing TI's SmartReflex™ technology with option for integrated and discrete Power Management ICs

Features

Cores

- Cortex A-8 with NEON™ SIMD Coprocessor / DSP-based TMS320C64x+ DSP and video accelerators (max performance only)
  - 600 MHz / 430 MHz @ 1.35V *(operating limits apply)*
  - 550 MHz / 400 MHz @ 1.27V
- 2D/3D Graphics Engine - Up to 10M polygons per second

Memory

- ARM:
  - 16 kB I-Cache; 16 kB D-Cache; 256kB L2
- TMS320C64x+ DSP and video accelerators
  - L1 32kB Program Cache/32kB Data Cache + 48kB SRAM
  - L2 64kB Program / Data Cache + 32 kB SRAM; 16 kB ROM
- On Chip: 64kB SRAM; 112kB ROM

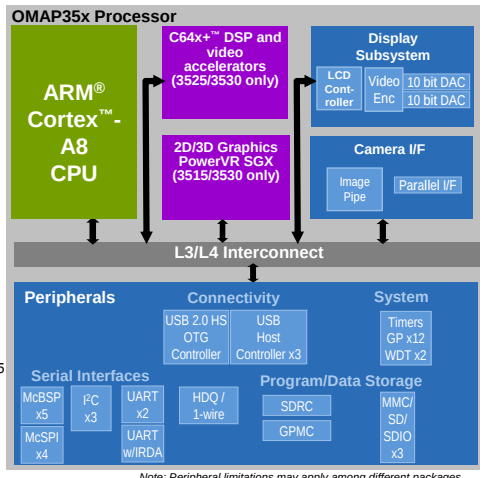
Peripheral Highlights

- Support for LPDDR
- Support for NOR, NAND, SRAM, Pseudo SRAM
- USB 2.0 HS Compliant OTG Controller w/ 2 additional USB Host Controllers
- Display subsystem with LCD and TV interface. Supports PIP, color space conversion, resize and rotation.
- Camera I/F with CCD controller and Image-pipe (Preview, Resize, Statistics

- Package 1 (CBB): 12x12 mm, 0.4mm pitch, Package On Package (POP); 515 pin PBGA; samples now; production 4Q'08; can be used with discrete memory
- Package 2 (CUS): 16x16 mm 0.65 mm pitch. 423 pin PBGA; samples now; production 4Q'08. Utilizes Via Channel™ Array Technology with 0.8mm pitch plus design rules.
- Package 3 (CBC): 14x14 mm, 0.5 mm pitch POP; 515 pin PBGA; samples Sep '08; production 1Q'09; must use POP memory

Applications include:

- Automotive Infotainment
  - In-dash navigation
- Consumer
  - PND
  - PMP
  - Digital Video Camera
- Medical
  - Patient monitoring
  - Portable ultrasound
- Industrial
  - Point of sale
  - Smart white goods



Note: Peripheral limitations may apply among different packages

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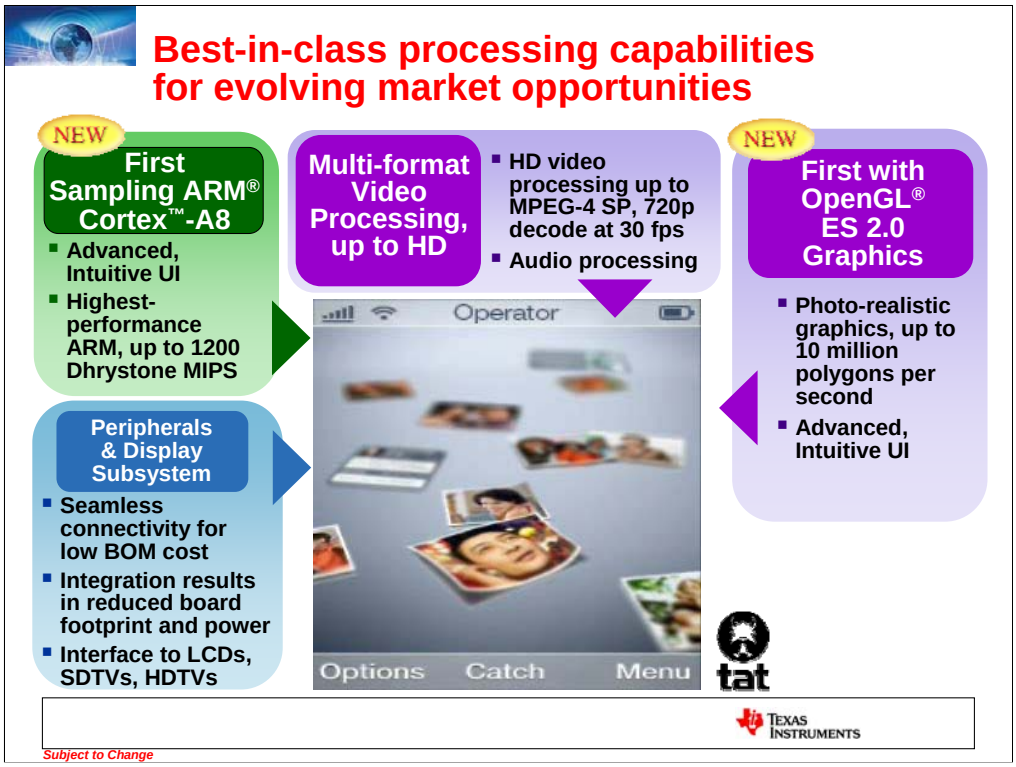
•Notes:

- •Block diagram components are "clickable" to provide additional information on each section
- •It should be stressed to the customer that manufacturing with 0.4mm ball pitch can be very challenging.
- •Customer should discuss with TI before starting a design intending to use .4mm and POP



•To summarize:

- •OMAP35x offers the first generally available CortexA8 solution. It achieves up to 1200 DMips and is roughly 4x the performance of an ARM9.
- •The c64x+ based video subsystem is capable of processing up to 720 HD resolution video.
- •This is the first generally available, integrated SOC that included OpenGL ES 2.0 compatible graphics hardware. This is capable of running up to 10 M polygons per second.
- •The highly integrated peripheral set includes many system level components that will reduce the overall BOM and PCB size

OMAP35x EVM, tools, and software

Begin development today with extensible OMAP35x evaluation module

Hardware

- OMAP35x Processor for evaluating all four OMAP35x devices
- 128 MB LPDDR/128 MB oneNAND Flash (or similar capacity and function)
- Touch screen LCD display
- Landscape/Portrait modes

Software

- OMAP3503 Linux BSP:
  - Kernel 2.6.22
  - Peripheral drivers
  - U-boot for boot loading
  - Busybox based root file system
- Windows® CE 6.0 BSP available 3Q08

[1] *Additional tools support from Microsoft, ARM, GreenHills, MontaVista, Lauterbach, and TI(CCS) will be made available in the future*

- **Evaluate capability**
- **Begin SW development**
- **Use Daughter card expansion to prototype complete system**
- **Easy to Upgrade to New Processors and Power Management Devices**

More information available at
www.ti.com/omap35x

Connectivity

- Daughter card connectivity
- Ethernet, USB 2.0, SDIO, I^2C, JTAG, Keypad
- SD/MMC
- S-Video output

Development tools and support[1]

- Code Sourcery Toolchain
- Reference schematics
- Emulator support: TI XDS560

OMAP35x EVM
TMDXEVM3503
$1495

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•To facilitate rapid development TI is offering the OMAP35x EVM.

•This board is based on OMAP35x silicon and includes a VGA touch screen LCD and 128 MB of LPDDR and 128 MB of oneNAND memory (utilizes POP technology) – memory may be second sourced over time, but this is the minimum capacity that will be offered

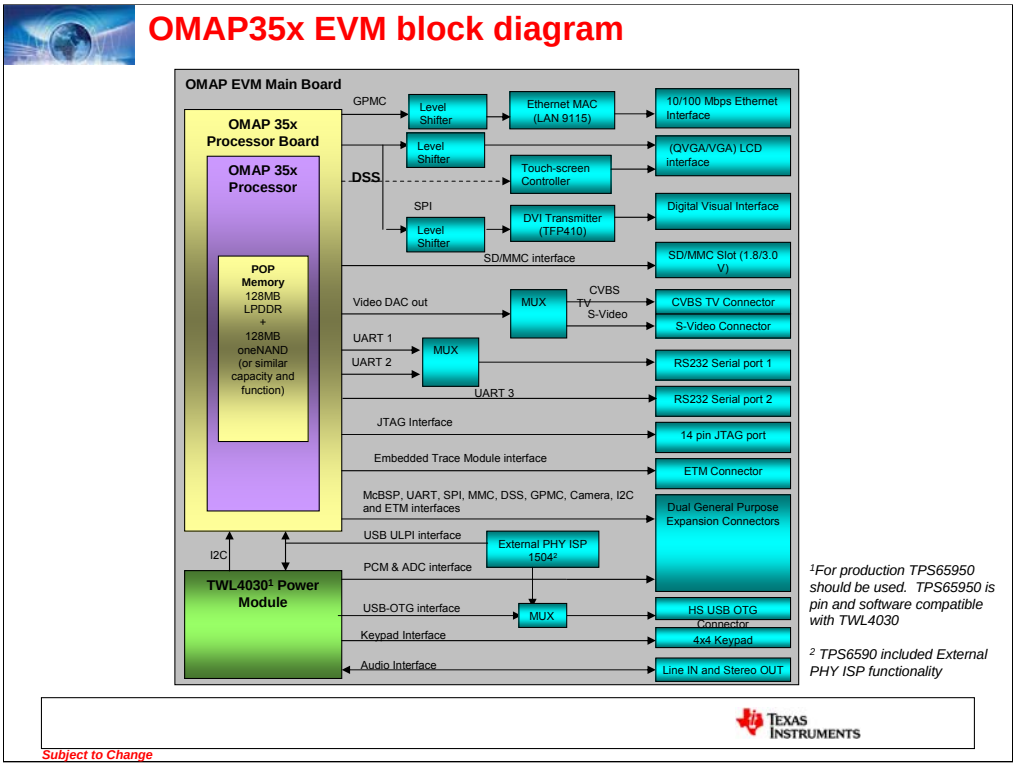
•The EVM is shipping today and includes non commercial Linux OS and drivers along with Code Sourcery tools.

•Reference schematics and Gerbers are available

•This board can be used to evaluate OMAP3503, OMAP3515, OMAP3525, and OMAP3530 silicon

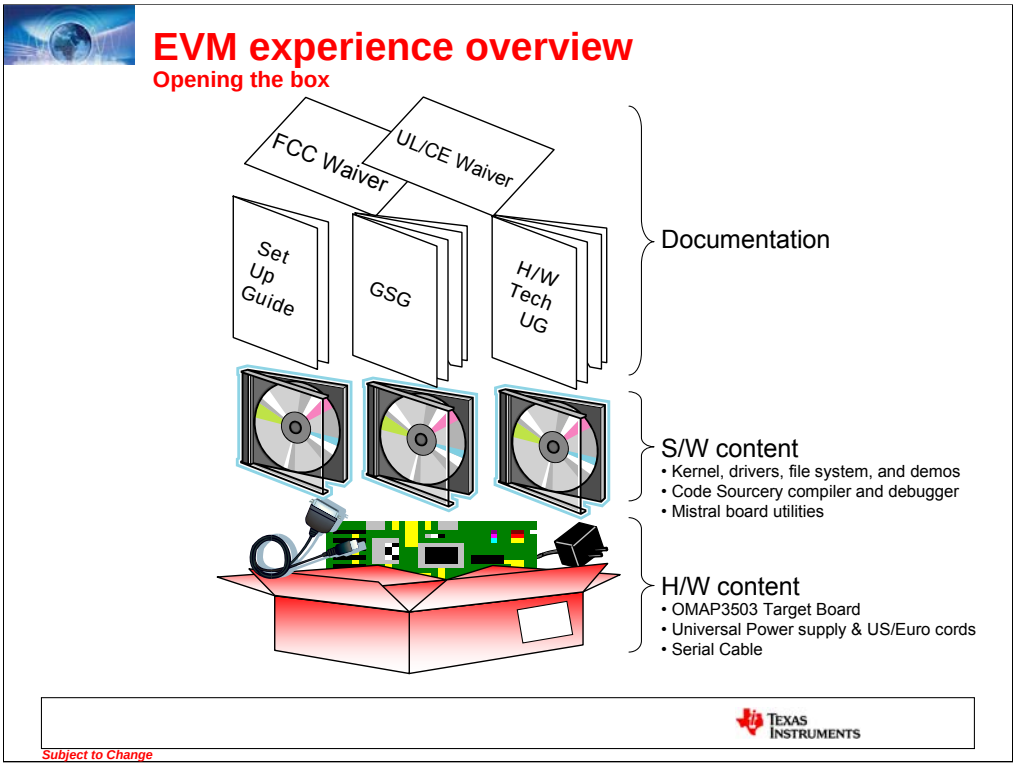
•Additionally WinCE will be made available via software download

•The basic OS and drivers for WinCE, when available, and Linux are offered in source code. No additional licensing fee or royalty is required to TI for use of the code (WinCE requires MSFT license)



•The OMAP35x EVM is based on a three boards to allow easy upgrading and development of power management solutions

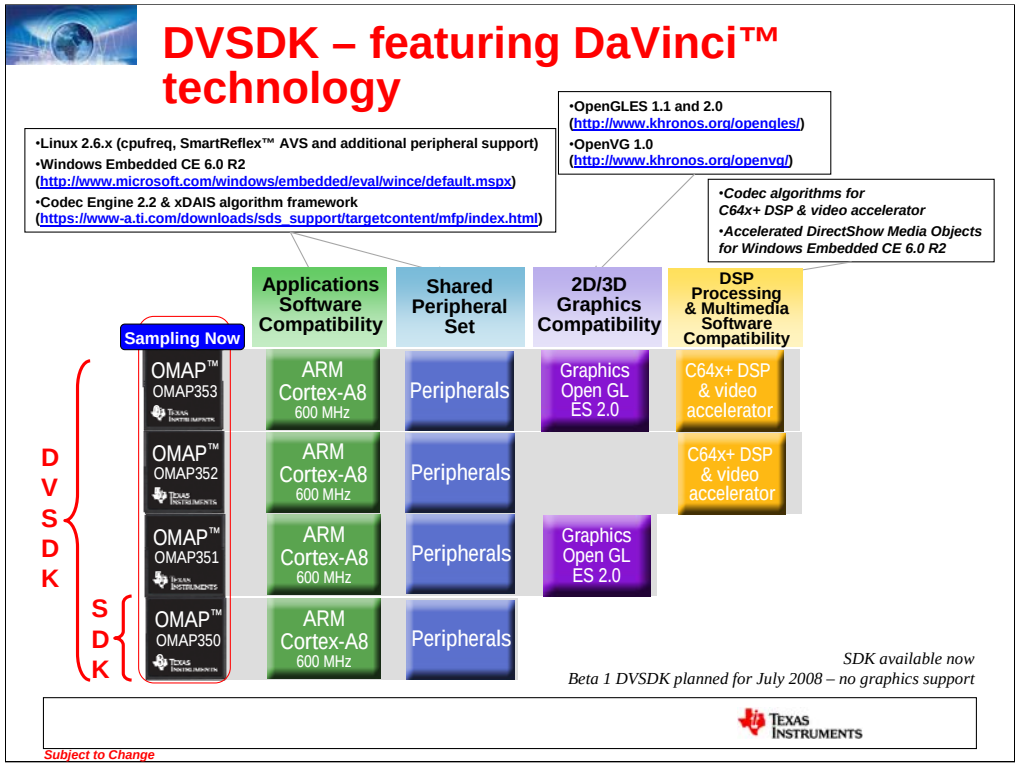
- •The base board, shown in gray, contains all the peripherals, expansion connectors, etc.
- •Connected to this is a processor board shown in yellow. This includes the OMAP35x device (0.4mm pitch) and stacked, POP memory
- •The third board is the power management board. This board is based on the TWL4030 device. TWL4030 is a preproduction device to the TPS65950. TPS65950 is pin and software compatible with the TWL4030



•This is a high level summary of what will be included in OMAP35x EVM

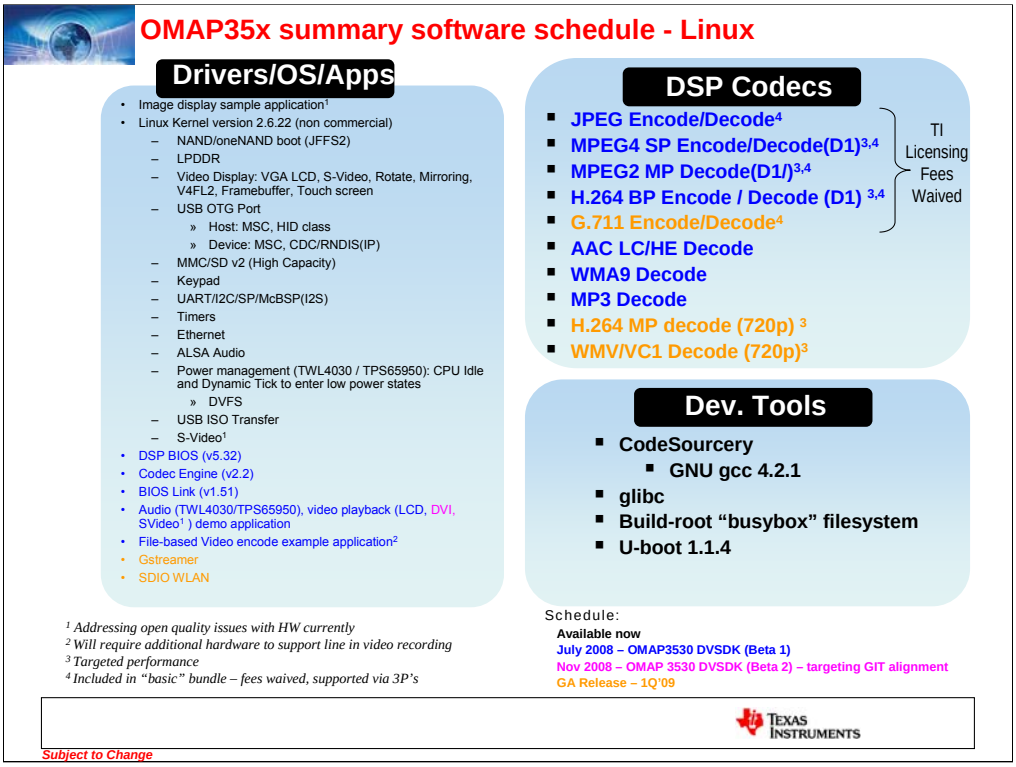
•All software and documentation will be available on the EVM update site.

•It is important that customers register their EVM and download the latest update when getting started

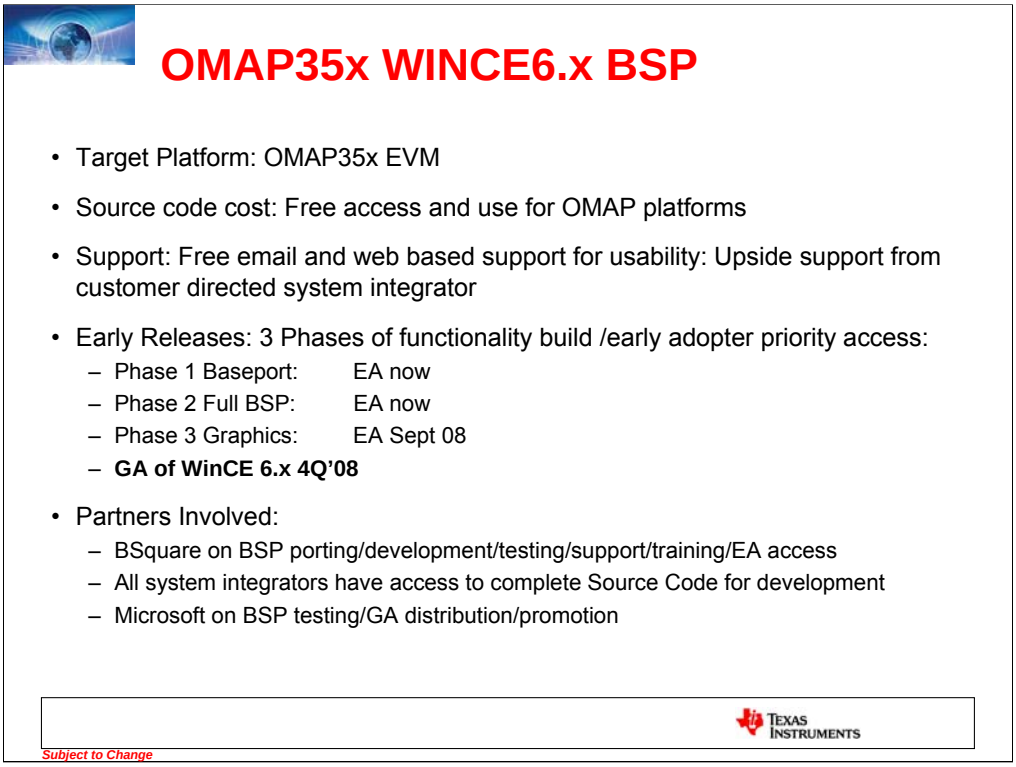


•The available SDK available covers the ARM and peripheral drivers only but is usable across all devices.
•Moving forward, the DVSDK featuring DaVinci technology to enable video on the OMAP3530 and OMAP3525 will support all four devices in the platform.
•The DVSDK will extend the current Linux support that is included in the SDK

- It will also add in support for WinCE 6.0 SR2
- It will be based on Codec Engine 2.2 and utilize our standard API libraries for enabling algorithms



•This slide provides additional granularity on the codecs that will be included in the DVSDK as well as drivers, OS, etc.



•WinCE development is targeted for the OMAP35x EVM

•This package will be available to all OMAP35x EVM customers at no charge with limited support

- •Additional support packages will be available from BSquare and other ecosystem partners

•Early adopter releases are available – contact the your OMAP35x BDM for information on this

- •These EA releases will be delivered directly from BSquare and will require execution of an evaluation agreement with BSquare

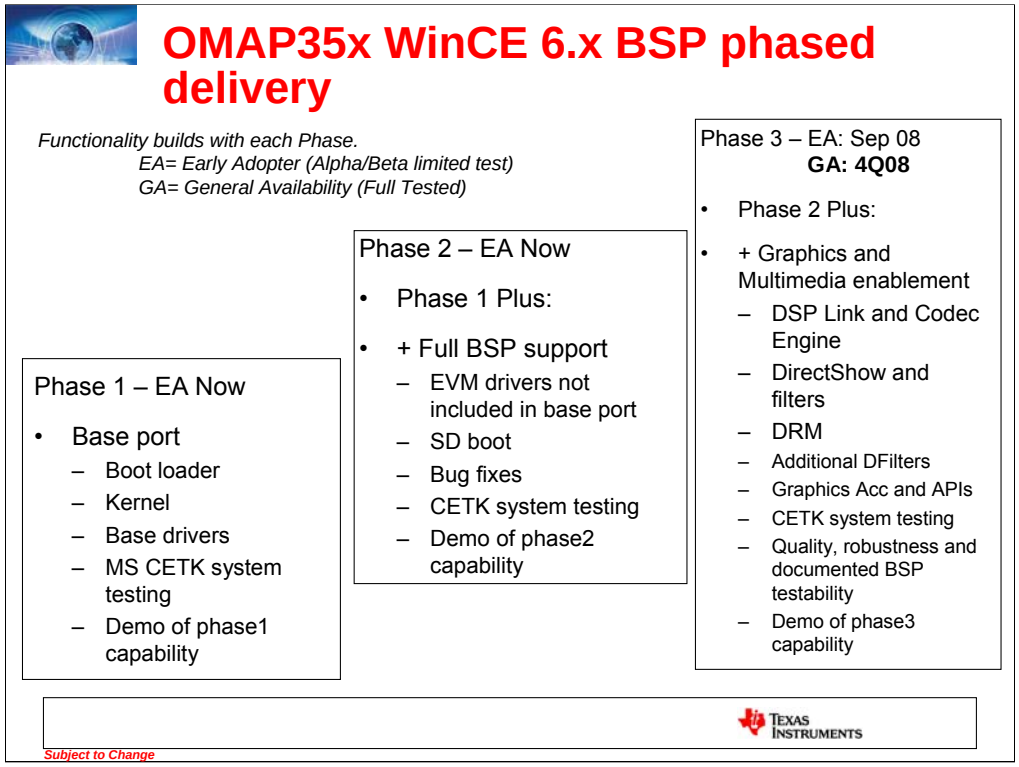
•Tools information:

From bSquare (~$1000):
http://www.bsquare.com/store/home.asp?CFID=5175554&CFTOKEN=12512615

Local distributors:
http://www.microsoft.com/windows/embedded/partners/find/distributors/search.mspx

Evaluation package (180 days) for free from MSFT:
http://www.microsoft.com/windows/embedded/downloads/default.mspx

CD's of evaluation package are also available:
https://ms.kpcorp.com/WinEmbedded/AspxFiles/Home.aspx



•OMAP35x will have support for WinCE 6.0 SR2

•The development will be a phased development as indicated.

•Code will be available at no charge for customers who have purchased the EVM

•Limited support will be included free with the EVM. Additional support packages will be available

Base drivers for WinCE delivery

- WaveForm Audio with IN and OUT support.
- LCD.
- Display with TV, S-Video Out, DVI support.
- Screen rotation support.
- Backlight
- Keypad
- Touchscreen
- Watchdog
- Debug UART
- Application UART
- Ethernet KITL
- USB KITL
- High Speed MMC/SD/SDIO
- High Speed USB.0 with OTG support
- RNDIS support for USB
- High Speed I2C
- TWL4030 (customers will need to switch to TPS65950 for production)
- GPIO
- DMA
- McBSP
- OneNAND Flash
- SPI
- Timers
- NLED Driver
- High Speed Timer

Support for industry's popular software tools

Tool / Top features	Debug	Compile	Other
Code Composer Studio™ IDE Platinum Edition	Low-level ARM and DSP	Low-level ARM (ARMv7) and DSP (NEON roadmap)	Power-aware debug
RealView Tools by ARM	Low-level ARM	Application-level ARM (ARMv7, NEON)	
Microsoft	WinCE application debug	WinCE ARM (ARMv7, NEON roadmap)	
LAUTERBACH	Low-level and app ARM and DSP	none	Extensive trace
montavista	Linux application debug	Linux kernel/app ARM	
Green Hills SOFTWARE, INC.	Low-level and app ARM and DSP	Low-level ARM	Trace
CodeSourcery	Linux application debug	Linux kernel/app ARM (ARMv7, NEON)	

•Cortex-A8 uses ARMv7 instructions

Additional third party information: here

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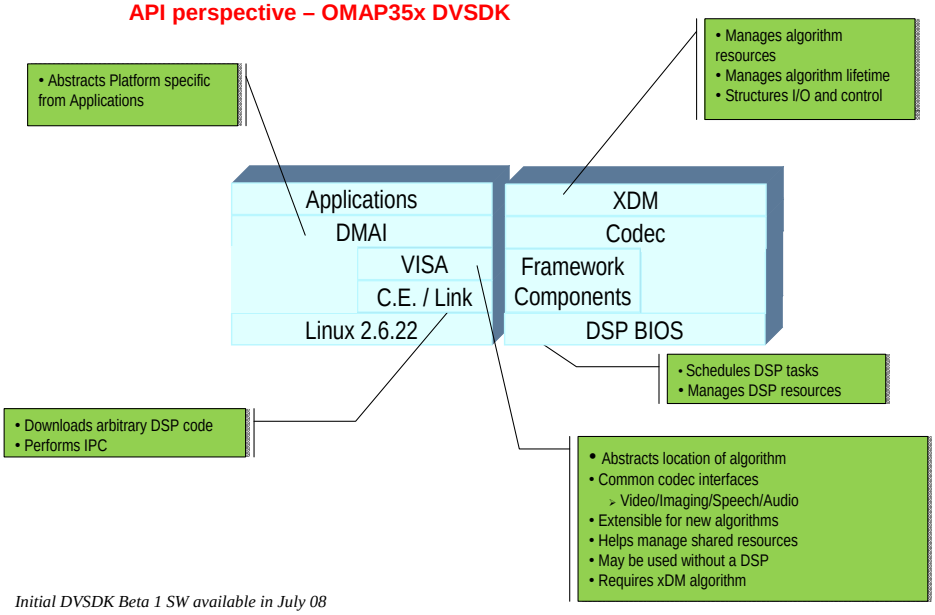
•TI's initial software includes CodeSourcery tools

•Other tools vendors support is either available or in progress

Overview of SW stacks

API perspective – OMAP35x DVSDK



Initial DVSDK Beta 1 SW available in July 08

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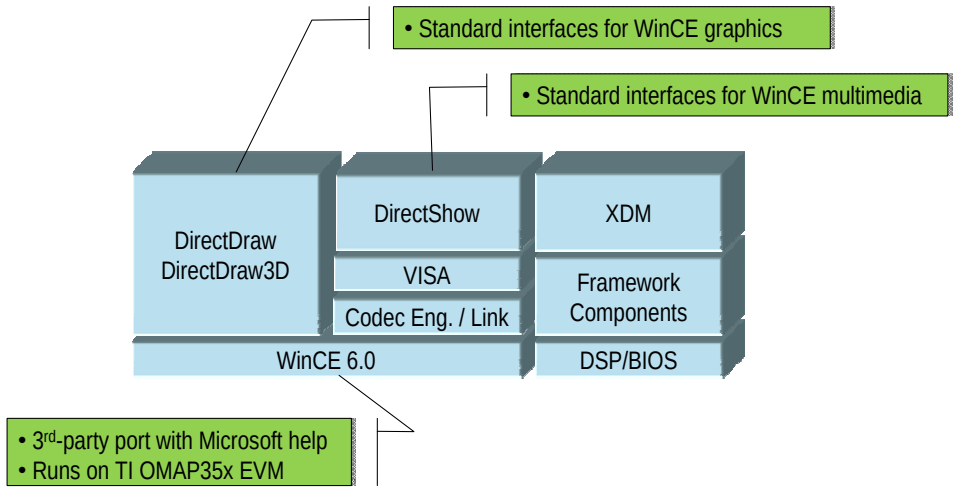
Overview of SW stacks

API perspective - WinCE



Codec and applications blocks omitted for simplicity

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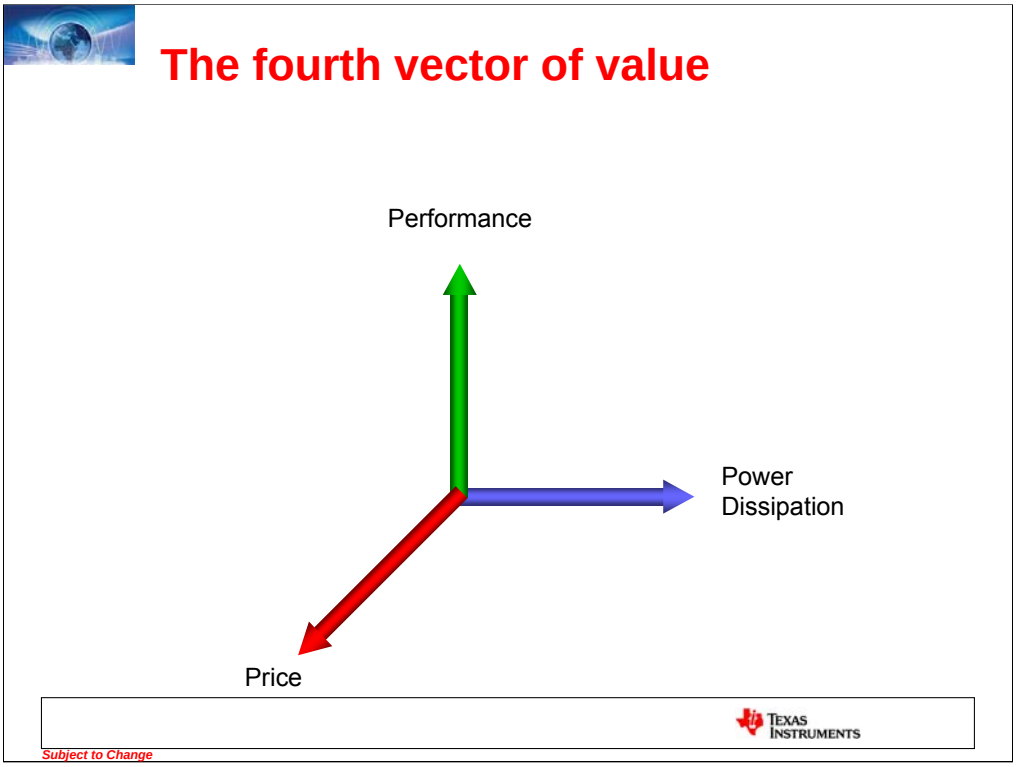
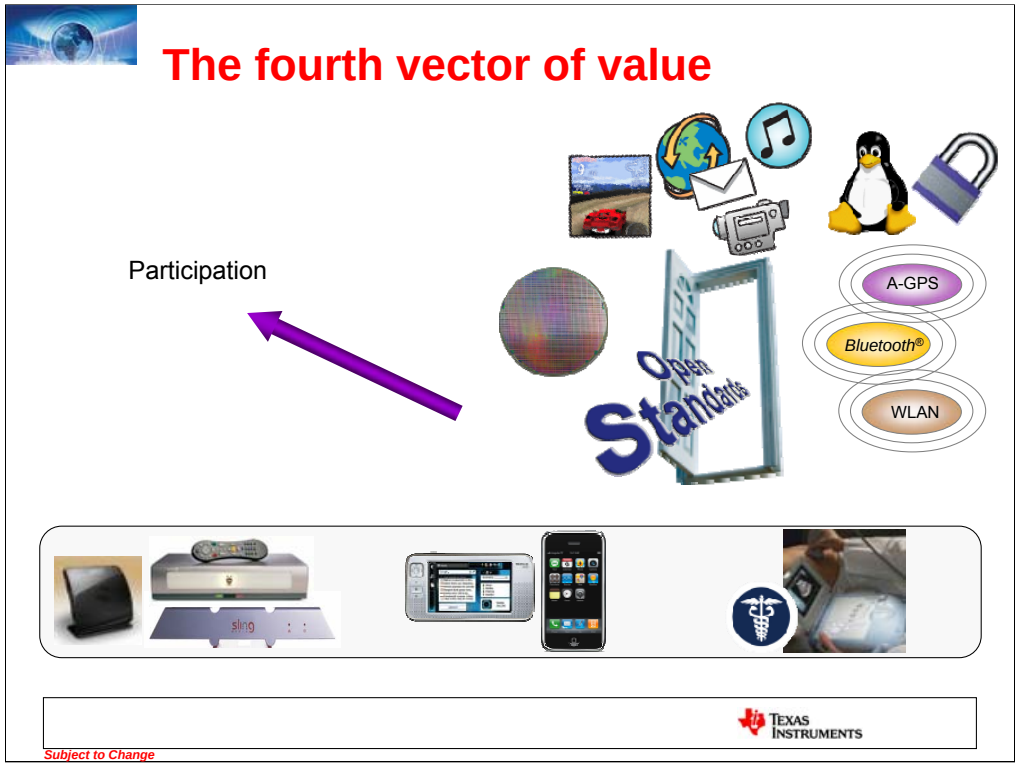
OMAP35x and open source



•There are several vectors to value of a solution: price, performance, and power dissipation.

•While software is not explicitly called out it is inherent to the performance, price and power dissipation vectors

•However, there is a fourth vector…



•A fourth vector of value is participation. Through participation, largely via software, the overall value of a solution can be increased.

General benefits of open source

- Faster Innovation
  - Collaborate faster than standard product release cycles
  - Engage and fuel passionate innovators/developers
  - Peer-to-peer conversation and open idea exchange
- Better Solutions
  - Software quality through expert peer review
  - New preferred peer support through community
  - Faster feedback on product requirements and tools

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•One of the easiest ways to encourage participation is open source software.
•Through the use of open source code and participation TI can enable faster innovation and better solutions on OMAP35x.

Why do people participate?

Simplified view

- Leverage community to solve own problems, then share for possible benefits
  - May develop solution on their own
  - Benefits are generally improvements to the code
  - Not much benefit required, if no expecting loss
  - May utilize community to various degrees

- Solve community problems for fame and glory
  - Could just like getting a “pat on the back”
  - Could get a job or contract

TI in open source devices

http://opensource.ti.com

- Neuros open source devices
  http://www.neurostechnology.com
- Nokia Internet tablets
  http://www.maemo.org
- OMAP™ 3…
  - Pandora handheld gaming devices
    http://www.openpandora.org
  - Zoom mobile development kit (cell phone focus)
    http://www.omapzoom.org/
  - Beagle board low-power, low-cost computer
    http://beagleboard.org

Beagle is…

- A low-power, low-cost, open source, bring-your-own-peripherals computer
  - Entry point for embedded software design
  - For hobbyists, students, and experimenters
- TI engaged with open source developers on ARM+C64x devices
- Community supported OMAP35x based platform

What's in a name…

B ring your own peripherals

E ntry-level cost ($149 target)

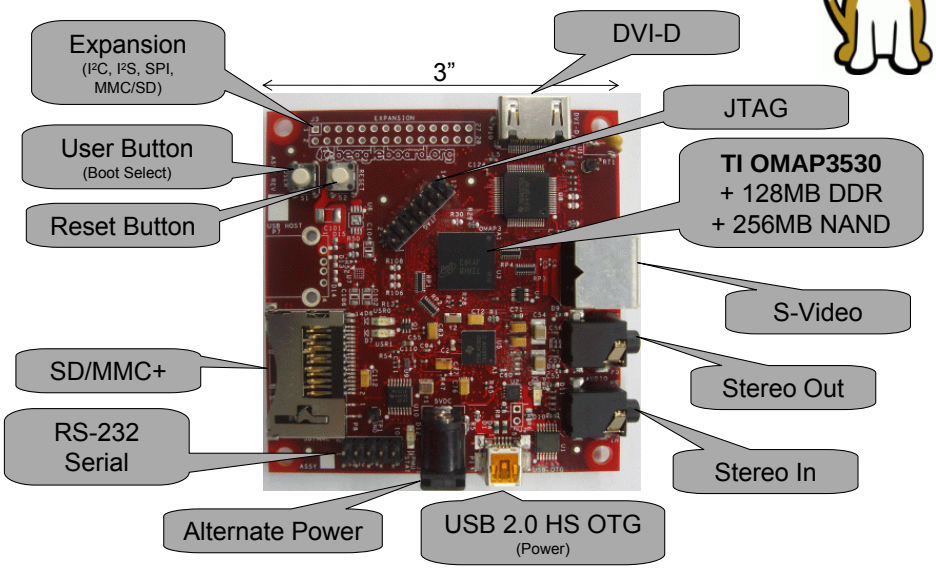
A rm Cortex-A8 (600MHz, superscaler)

G raphics and DSP / Video accelerated

L inux (and possibly even WinCE) ports

E nvironment for software innovators

The Beagle Board



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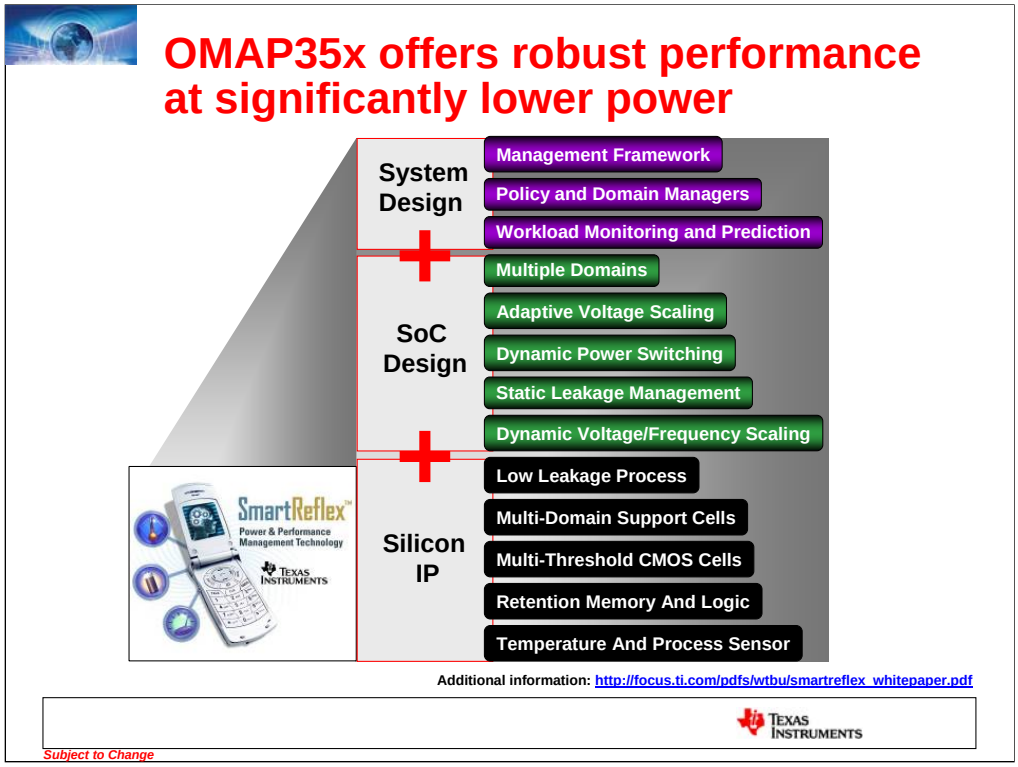
OMAP35x power and analog solutions

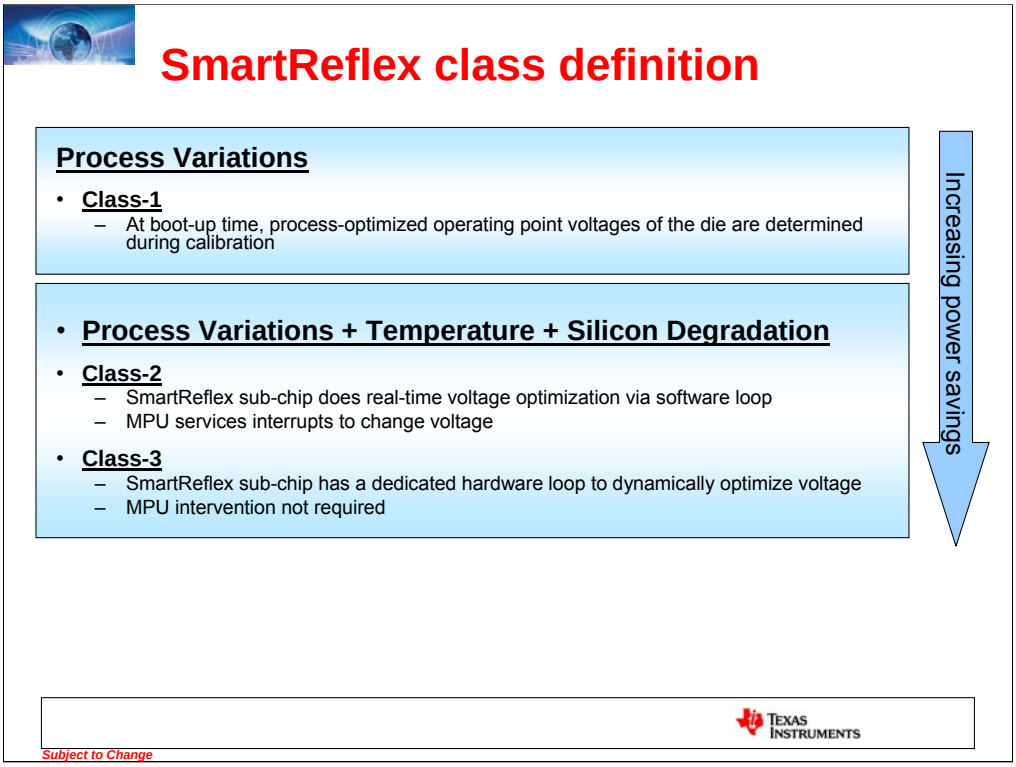


•TI's Smartreflex technology enables TI silicon to operate at low power levels while still being manufactured in increasingly smaller, and "leakier", process technologies

•This technology allows for a system to dynamically compensate for variations in temperature, manufacturing process, and silicon degradation over time to reduce voltage, gate off unused peripherals, and adjust clocks as needed all to lower power consumption.

•Three vectors are required to enable this:

- •Silicon IP
- •SoC (System on a chip) design
- •System design



•Before reviewing companion power offerings from TI it is important to understand some basic definitions associated with Smartreflex

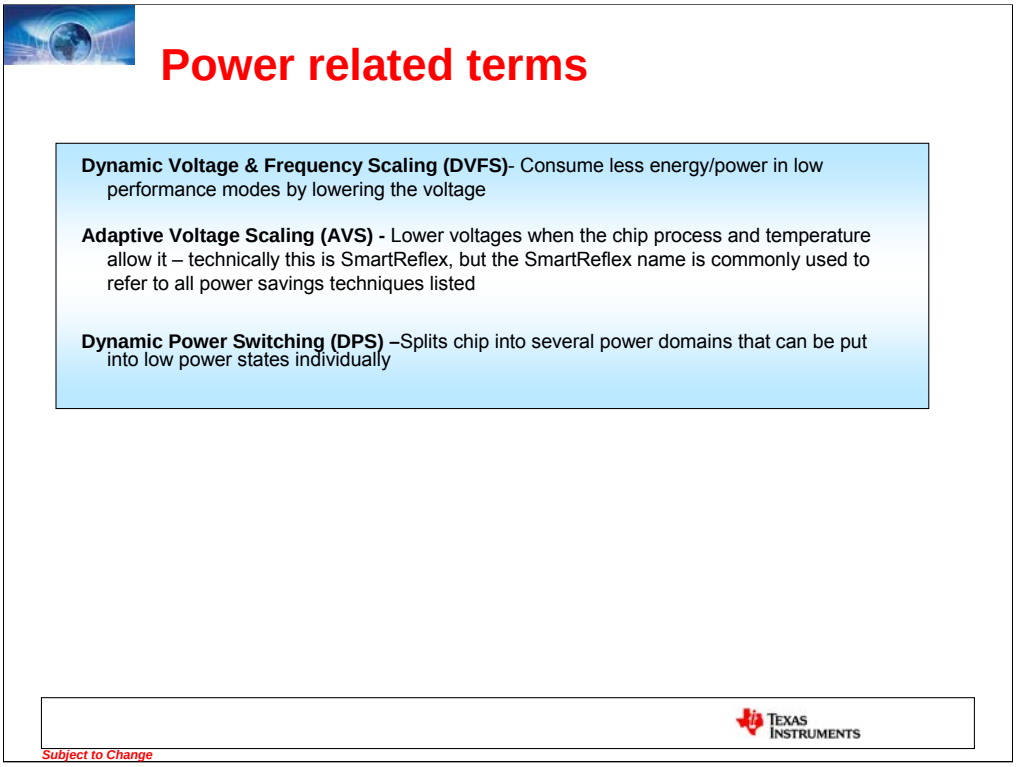
•The “class” associated with a companion power devices identifies to what extent Smartreflex technology can be uses

•There are three classes relative to OMAP35x

•Power savings increase with each subsequently higher class

•Class 1 and Class 2 are software based

•Class 3 is hardware based



•It is important to understand these terms before reviewing OMAP power solutions

•The term AVS can be a confusing. In technical circles this will be used interchangeably with Smartreflex. In the marketing and communication world, Smartreflex will refer to all the power management techniques

Power & analog companion options for OMAP35x

DVFS & Class-3 SmartReflex Capable

- **PMIC (multi-output DCDC)**
  - **TPS65950**[1] (July, RTM Sep 08)
  - **TPS65930** (Sep 08, RTM Dec 08)
  - **TPS65920** (Sep 08, RTM Dec 08)

DVFS & Class-2 SmartReflex Capable

- **PMIC (multi-output DCDC)**
  - **TPS65023**[2] (in production)
  - **TPS65073**[2,3] (samples Dec 08, RTM 1Q 09)
- **Single Output DCDC**
  - **TPS62350**[2,3] (in production)

[1] Software and pin compatible with TWL4030 [2] Driver availability 2H'08 [3] Support for Class-3 SmartReflex, under investigation

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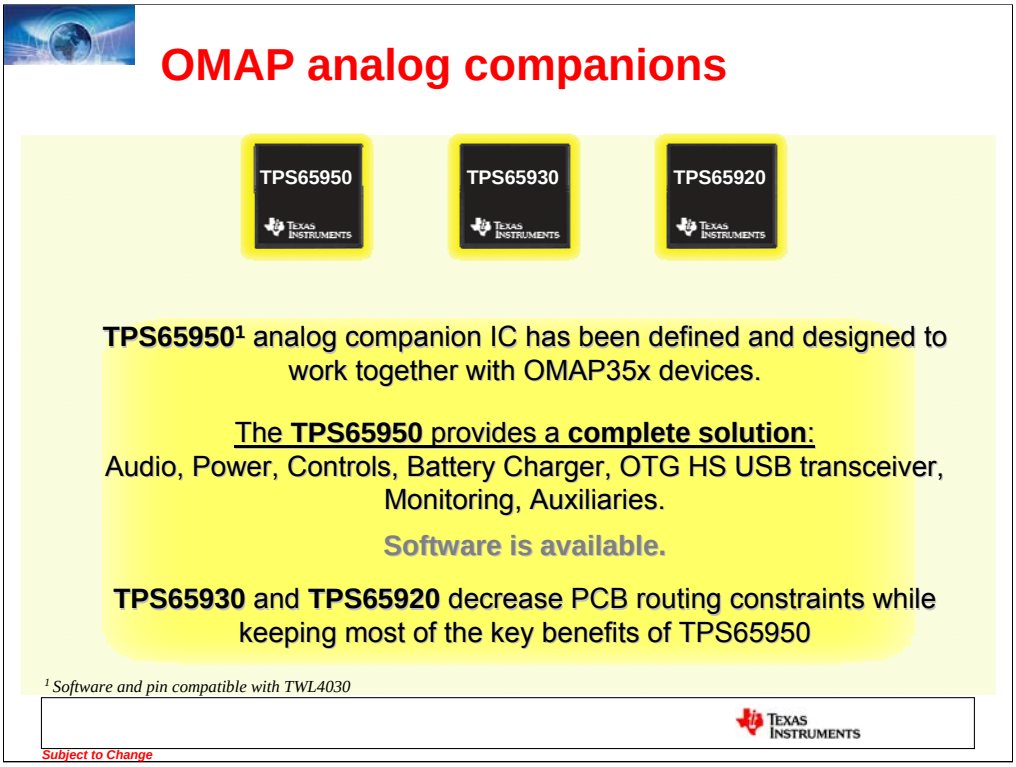
Part Numbering In General

TPS65 = TI Catalog Multi-Output PMU devices (>2 outputs)

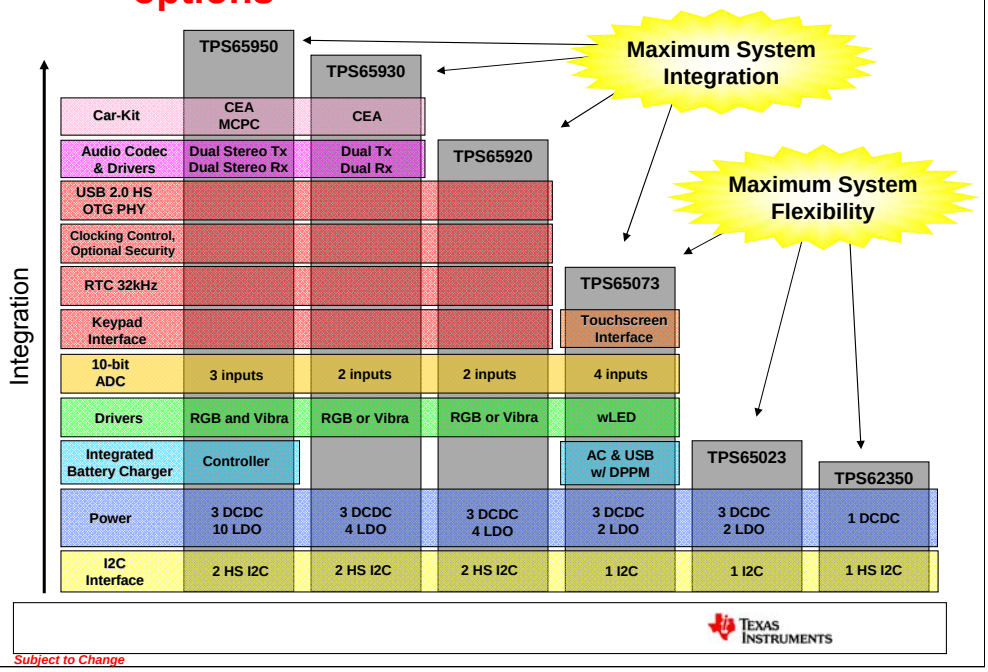
TPS62 = TI Catalog DCDC converters (≤2 outputs)



•TPS65950 is a pin and software compatible production replacement for the TWL4030 that is currently on the OMAP35x EVM.

•TPS65950 is 0.4mm ball pitch. TPS65930 and TPS65920 are 0.65mm ball pitch

Feature overview of OMAP35x power options



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www.ti.com/omap35x
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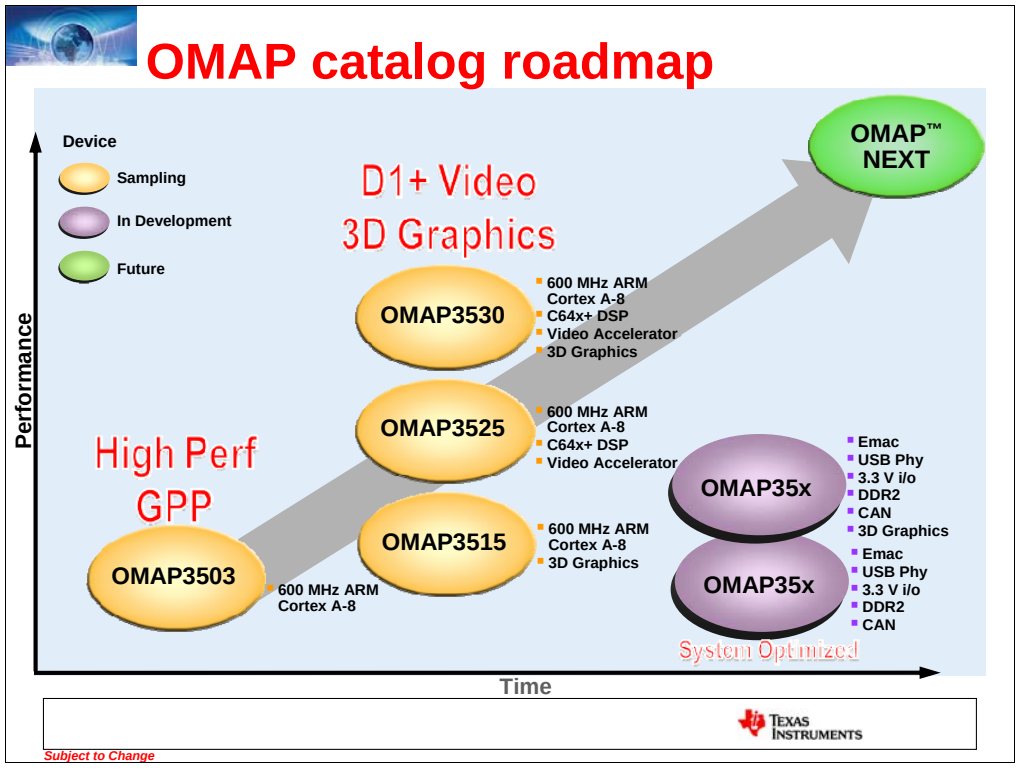


•OMAP3503 is the first in a line of OMAP35x solutions available to the general market it features a high performance Cortex A8

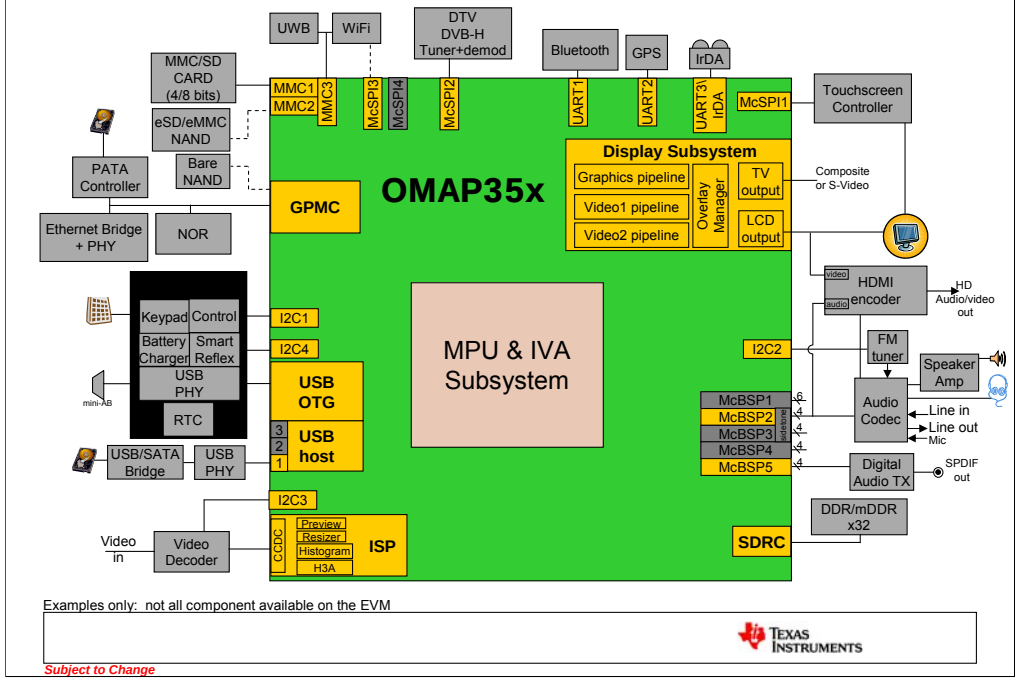
•OMAP3530, OMAP3525, and OMAP3515 are now sampling and include the Cortex-A8 as well as high performance graphics, DSP, and video accelerators as indicated.

•The OMAP35x devices in development are targeted to sample in 1H'09 and are include the added features shown. These devices will remain as close to software and pin compatible as possible given the changes. They will not be 100% pin or software compatible and will not be drop in replacements due to the peripheral changes.

- It is expected that these solutions will offer anywhere from $2-3 in system BOM savings to as much as $9 or $10 depending on the then current memory pricing and additional features utilized

•OMAP NEXT will improve on the performance of the ARM core, increase video performance and add significant peripheral integration for broad markets.

OMAP35x connectivity examples

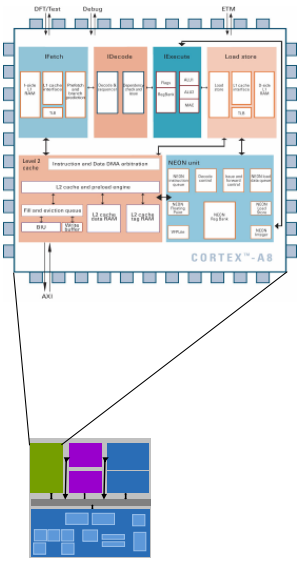


•This slide shows possible connectivity examples for a highly integrated end product.

•This is intended for discussion purpose only. Not all components are integrated on EVM, TI does not support drivers for all external components.

OMAP35x block diagram details

ARM Cortex™ - A8



- Up to 600 MHz
- ARMv7 Architecture
  - Thumb®-2
  - MMU Enhancements
- In-Order, Dual-Issue, Superscalar Microprocessor Core
- NEON™ Multimedia Architecture
  - Over 2x Performance of ARMv6 SIMD
  - Supports Both Integer and Floating Point
  - SIMD
- Jazelle® RCT Execution Environment Architecture
- Dynamic Branch Prediction with Branch Target Address Cache, Global History Buffer, and 8-Entry Return Stack
- Embedded Trace Macrocell (ETM) Support for Non-Invasive Debug
- ARM Cortex™-A8 Memory Architecture:
  - 16K-Byte Instruction Cache (4-WaySet-Associative)
  - 16K-Byte Data Cache (4-Way Set-Associative)
  - 256K-Byte L2 Cache
- Endianess
  - Instructions: Little Endian
  - Data: Configurable

Additional information: http://focus.ti.com/lit/ug/sprufa0a/sprufa0a.pdf

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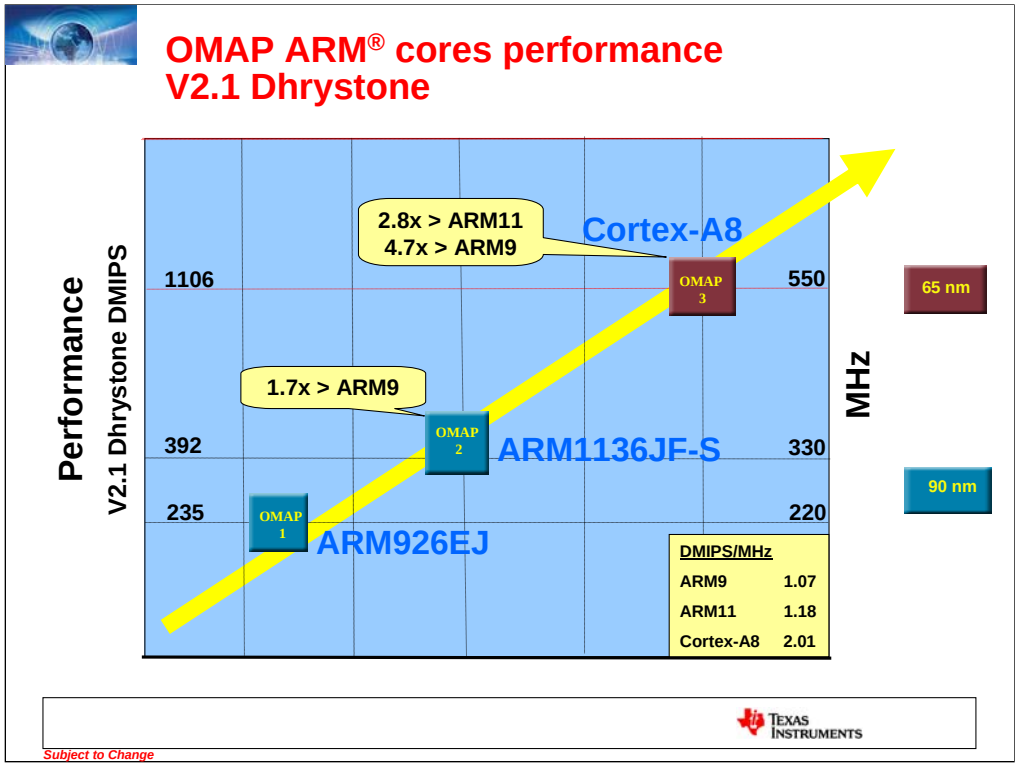
If additional information link does not work, please use this one: http://focus.ti.com/docs/prod/folders/print/omap3530.html#technicaldocuments and select the appropriate doc



•Dhrystone is a short synthetic benchmark (simple programs that are carefully designed to statistically mimic some common set of programs) program intended to be representative for system (integer) programming.

•The Dhrystone benchmark contains no floating point operations.

•Dhrystones per second is the metric used to measure the number of times the program can run in a second. Dhrystone tries to represent the result more meaningfully than MIPS (million instructions per second), because MIPS cannot be used across different instruction sets (e.g. RISC vs. CISC) for the same computation requirement from users. Thus, the main score is just

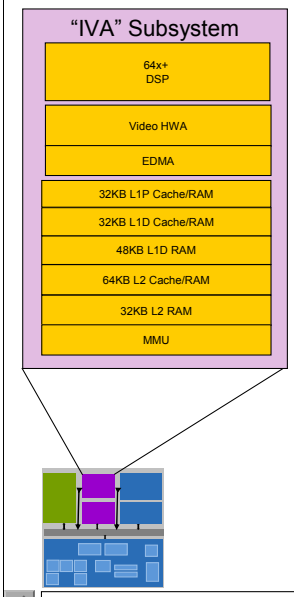
•Dhrystone loops per second. Another common representation of the Dhrystone benchmark is the **DMIPS** - Dhrystone MIPS - obtained when the Dhrystone score is divided by 1,757 (the number of Dhrystones per second obtained on the VAX 11/780, nominally a 1 MIPS machine).

Cortex naming – the basics

- There are several Cortex versions. How is the Cortex A8 differentiated?
- ARM Cortex
  - Cortex A – Applications
    - High Performance, Full OS, Low Power
  - Cortex R – Real-Time
    - Embedded Processing, real-time
  - Cortex M – Microcontroller
    - Cost sensitive embedded applications
- OMAP35x is the world's first general available A8

Additional information: http://www.arm.com/products/CPUs/families/CortexFamily.html

C64x+™ DSP and accelerators



- Up to 430 MHz (c64x+ DSP)
- Dedicated enhanced data memory access (EDMA) engine to download/upload data from/to memories and peripherals external to the sub-chip
- Video hardware accelerators
- MMU to access external address space (such as memory/peripheral)
- Dedicated interrupt controller, DPLL, WUGEN and SYSC modules
- Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x+™ DSP Core
  - Eight Highly Independent Functional Units
    - Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle
    - Two Multipliers Support Four 16 x 16-B Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-B Results) per Clock Cycle
  - Load-Store Architecture With Non-Aligned Support
  - 64 32-Bit General-Purpose Registers
  - Instruction Packing Reduces Code Size
  - All Instructions Conditional
  - Additional C64x+™ Enhancements
    - Protected Mode Operation
    - Exceptions Support for Error Detection and Program Redirection
    - Hardware Support for Modulo Loop Operation
- C64x+ L1/L2 Memory Architecture
  - 32K-Byte L1P Program RAM/Cache (Direct Mapped)
  - 80K-Byte L1D Data RAM/Cache (2-Way Set-Associative)
  - 64K-Byte L2 Unified Mapped RAM/Cache (4-Way Set-Associative)
  - 32K-Byte L2 Shared SRAM and 16K-Byte L2 ROM
- C64x+ Instruction Set Features
  - Byte-Addressable (8-/16-/32-/64-Bit Data)
  - 8-Bit Overflow Protection
  - Bit-Field Extract, Set, Clear
  - Normalization, Saturation, Bit-Counting
  - Compact 16-Bit Instructions
  - Additional Instructions to Support Complex Multiplies
- Little Endian

Additional information: http://focus.ti.com/lit/ug/sprufa3a/sprufa3a.pdf

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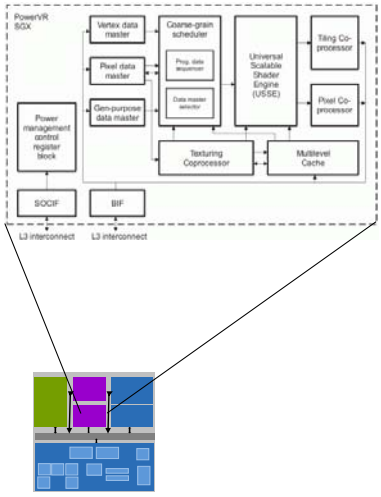
PowerVR SGX graphics engine



- **Up to ~111 MHz**
- **Tile Based Architecture Delivering up to 10 MPoly/sec**
- **Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality**
- **Industry Standard API Support: OpenGLES 1.1 and 2.0, OpenVG1.0 and Direct3D Mobile**
- **Fine Grained Task Switching, Load Balancing, and Power Management**
- **Programmable High Quality Image Anti-Aliasing**

Additional information: http://focus.ti.com/lit/ug/spruff6a/spruff6a.pdf
Graphics white paper: http://focus.ti.com/lit/wp/spry110/spry110.pdf

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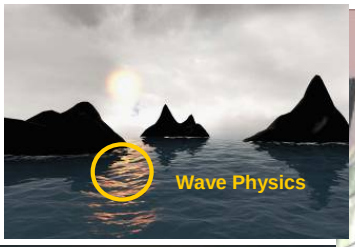
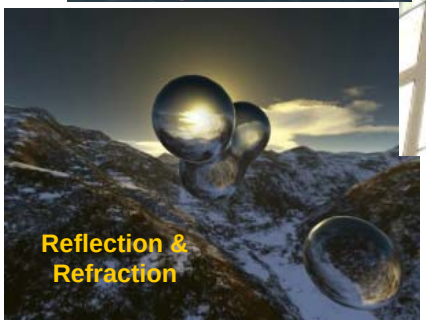
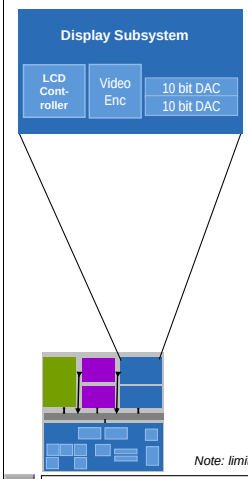
Graphics capability examples





Images provided by Imagination Technologies

Display subsystem (DSS)



- **Parallel Digital Output**
  - **Up to 24-Bit RGB**
  - **HD Maximum Resolution**
  - **Supports Up to 2 LCD Panels**
  - **Support for Remote Frame Buffer**
  - **Interface (RFBI) LCD Panels**
- **2 10-Bit Digital-to-Analog Converters(DACs) Supporting:**
  - **Composite NTSC/PAL Video**
  - **Luma/Chroma Separate Video (S-Video)**
- **Rotation 90-, 180-, and 270-degrees**
- **Resize Images From 1/4x to 8x**
- **Color Space Converter**
- **8-bit Alpha Blending**

Note: limitations may apply among packages

Additional information: http://focus.ti.com/lit/ug/sprufa4/sprufa4.pdf

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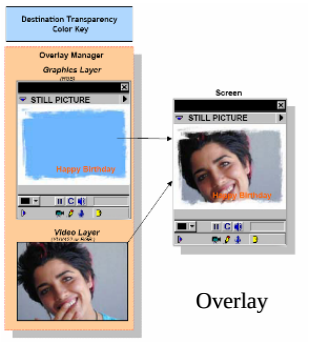
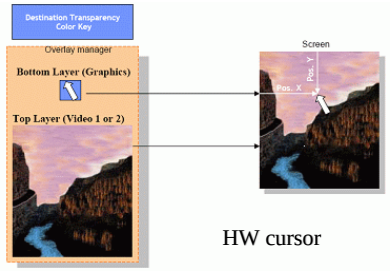
Display subsystem examples

PiP

Scaling



Overlay



HW cursor

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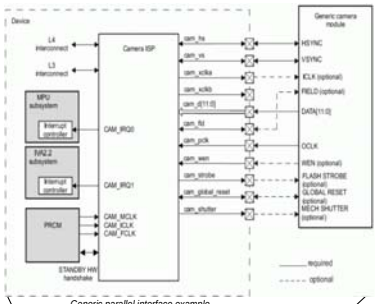
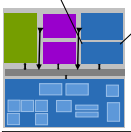
Camera interface subsystem (ISP)



Generic parallel interface example

- CCD and CMOS Imager Interface
- Memory Data Input
- RAW Data Interface
- BT.601/BT.656 Digital YCbCr 4:2:2 (8-/16-Bit) Interface
- A-Law Compression and Decompression
- Preview Engine for Real-Time Image Processing
- Glueless Interface to Common Video Decoders
- Histogram Module/Auto-Exposure, Auto-White Balance, and Auto-Focus Engine
- Resize Engine
  - Resize Images From 1/4x to 4x
  - Separate Horizontal/Vertical Control



Note: limitations may apply among packages

Additional information: http://focus.ti.com/lit/ug/sprufa2/sprufa2.pdf

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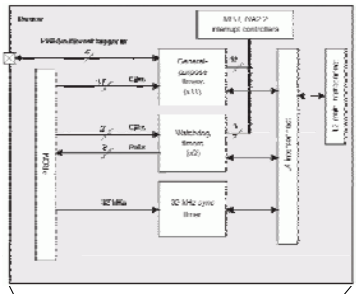
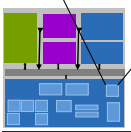
Timers



- **12 32-bit General Purpose Timers**
- **2 32-bit Watchdog Timers**
- **1 32-bit 32-kHz Sync Timer**



Note: limitations may apply among packages

Additional information: http://focus.ti.com/lit/ug/sprufa9a/sprufa9a.pdf

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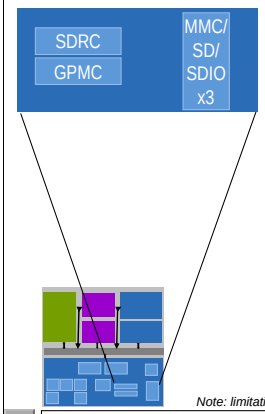
SD / MMC, SDRC, and GPMC interface

- **SD / MMC / SDIO**
  - Three instantiations
  - Compliant with CE-ATA and ATA for MMCA
  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards
- **General Purpose Memory Controller (GPMC)**
  - 16-bit Wide Multiplexed Address/Data Bus
  - Up to 8 Chip Select Pins With 128M-Byte Address Space per Chip Select Pin
  - Glueless Interface to NOR Flash, NAND Flash (With ECC Hamming Code Calculation), SRAM and Pseudo-SRAM
  - Flexible Asynchronous Protocol Control or Interface to Custom Logic (FPGA, CPLD, ASICs, etc.)
  - Nonmultiplexed Address/Data Mode Limited 2K-Byte Address Space)
- **SDRAM Controller (SDRCM) Subsystem**
  - 16, 32-bit Memory Controller With 1G-Byte Total Address Space
  - Interfaces to Low-Power Double Data Rate (LPDDR) SDRAM
  - SDRAM Memory Scheduler (SMS) and Rotation Engine



Note: limitations may apply among packages

Additional information:
SD/MMC: http://focus.ti.com/lit/ug/sprufd2a/sprufd2a.pdf
SDRC / GPMC: http://focus.ti.com/lit/ug/sprufa1a/sprufa1a.pdf

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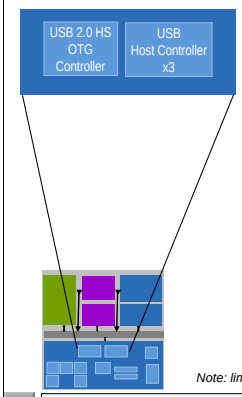
If additional information link does not work, please use this one: http://focus.ti.com/docs/prod/folders/print/omap3530.html#technicaldocuments and select the appropriate doc

USB

- **USB 2.0 HS OTG Controller**
  - USB 2.0 low-speed (1.5M bit/s), full-speed (12M bit/s), and high-speed (480M bit/s) host
  - USB 2.0 full-speed (12M bit/s), and high-speed (480M bit/s) peripheral
  - OTG Support
  - PHY interface – ULPI (HS/FS)



- **USB Host Controller**
  - Host only
  - All 3 ports operate in either HS or FS mode (determined by selected PHY connection)
  - HS Mode
    - 480M bit/s
    - Available Port – 1 & 2
    - PHY interface ULPI
  - FS Mode
    - 12M bit/s
    - Available Port – 1, 2, and 3
    - PHY interface Serial Asynchronous

Note: limitations may apply among packages

Additional information: http://focus.ti.com/lit/ug/sprufd4/sprufd4.pdf

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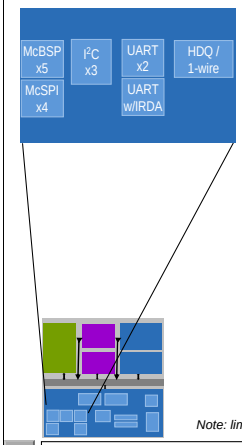
If additional information link does not work, please use this one: http://focus.ti.com/docs/prod/folders/print/omap3530.html#technicaldocuments and select the appropriate doc

Serial interfaces and HDQ/1-Wire

- 3 Master/Slave High-Speed Inter-Integrated Circuit Controllers (I²C)
- 5 Multi Channel Buffered Serial Ports (McBSP)
  - 512 Byte Transmit/Receive Buffer (McBSP1/3/4/5)
  - 5K-Byte Transmit/Receive Buffer (McBSP2)
  - SIDETONE Core Support (McBSP2 and 3 Only) For Filter, Gain, and Mix Operations
  - Direct Interface to I2S and PCM Device and TDM Buses
  - 128 Channel Transmit/Receive Mode
- 4 Master/Slave Multi Channel Serial Port Interface (McSPI)
- 3 UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)
- 1 HDQ / 1-Wire



Additional information:
I2C: http://focus.ti.com/lit/ug/sprufc6/sprufc6.pdf
McBSP: http://focus.ti.com/lit/ug/sprufd1a/sprufd1a.pdf
McSPI: http://focus.ti.com/lit/ug/sprufc9/sprufc9.pdf
UART: http://focus.ti.com/lit/ug/sprufc5/sprufc5.pdf
HDQ: http://focus.ti.com/lit/ug/sprufd0/sprufd0.pdf

Note: limitations may apply among packages

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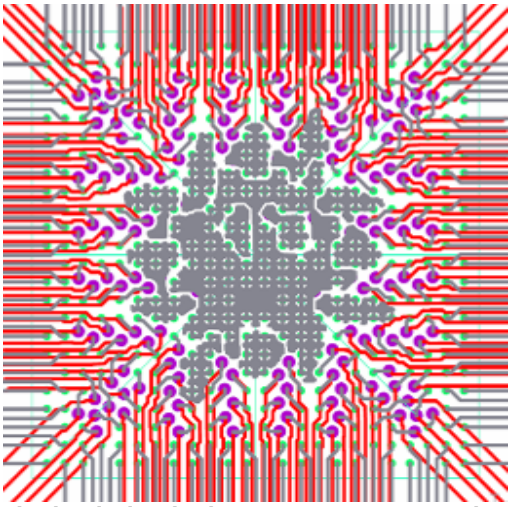
Via Channel™ array technology

Via Channel™ array solution – CUS package



Package Stats:
- **0.65mm pitch, BUT**
- **18 mil (0.45mm) vias**
- **5 mil (0.125mm) space/trace width**
- **2 layer routing**

Comparison with 0.8mm:
- **Requires fewer PCB layers**
- **Cheaper PCB cost due to reduced layers**
- **Bigger via size**
- **Same trace width**
- **Same space width**
- **Only assembly tolerances are tighter**

Final solution is the OMAP35x CUS package with 423 pins routed out in only 2 signal layers using 0.8mm+ pitch PCB rules.

Additional information: http://www.ti.com/litv/pdf/spraav6b

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- Normal 0.65mm Pitch Array Disadvantages:
  - Requires 4 mil traces/spaces (more expensive)
  - Requires 14-16 mil vias (more $$, reduced yield)
  - Not possible to use large 18 mil annular via rings for better yield
  - 10-15% more expensive than .8mm pitch BGA rules because of the above.

0.65mm pitch Via Channel™ packaging vs. 0.8mm pitch

Comparison	(Competition) 0.8mm pitch	(OMAP35x – CUS package) 0.65mm p. w/Via Channels
Micro Vias?	No	No
Min Trace	5 mils	5 mils
Min Space	5 mils	5 mils
Package size	17mm x 17mm (400 pins)	16mm x 16mm (423 pins)
Area	289mm^2	256mm^2
PCB Layers req.	6	4
Reduction from .8mm	--	11%

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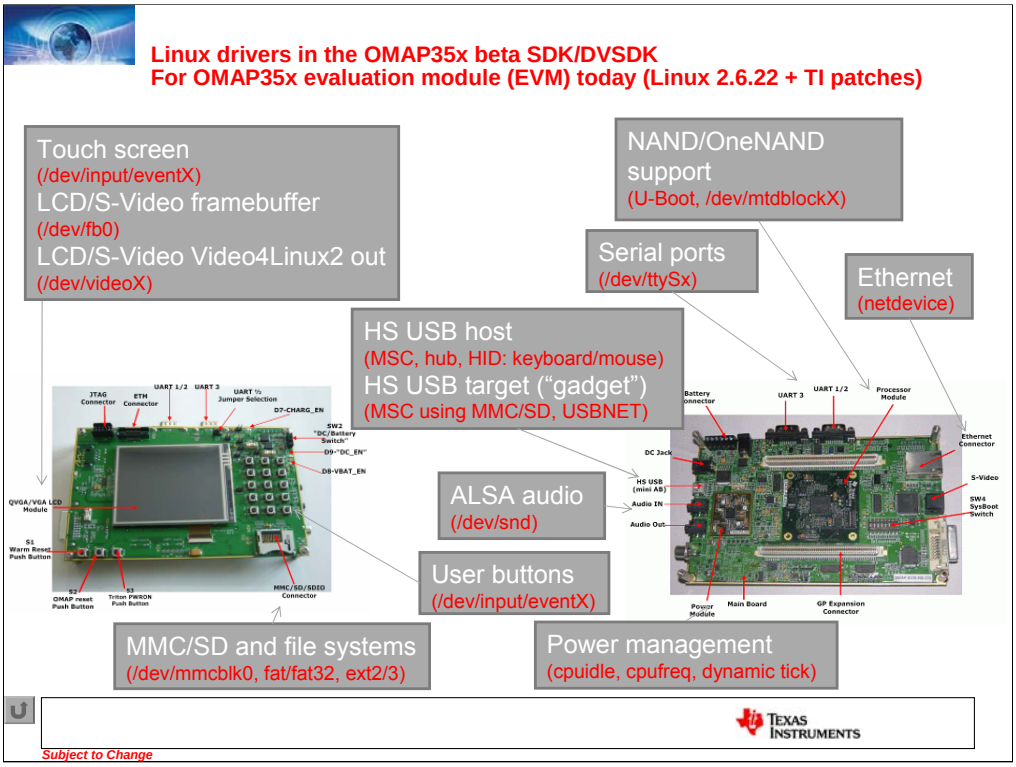
Conversion between mm and mils

- 0.075mm = 3 mils (0.003”) (actually 0.076mm)
- 0.1mm = 4 mils (0.004”) (0.102mm)
- 0.125mm = 5 mils (0.005”) (0.127mm)
- 0.2mm = 8 mils (0.008”) (0.203mm)
- 0.4mm = 16 mils (0.016”) (0.406mm)
- 0.45mm = 18 mils (0.018”) (0.457mm)
- 0.5mm = 20 mils (0.020”) (0.508mm)

OMAP35x tools



•This slides describes in details the drivers included in the OMAP35x software release

Common questions

OMAP35x preliminary power estimates

- MP3 Decode (DSP) – <30 mW[1]
- MPEG4 SP D1 Decode (on DSP/accelerators) – <390 mW[1]
- "Off Mode" – 477uW [2]
  - Lowest power mode from which OMAP35x can still wakeup autonomously
- "Standby 1" – 2.62mW [3]
  - Device state in which all non-Wakeup domains in the device are in low power retention
- ARM Cortex-A8 only – 0.52mA/MHz/V [4]

[1]Estimates are for OMAP35x only and are based on silicon models, with some correlation to measured data. Estimates assume room temp, overhead for Linux OS, and full utilization of DPS, DFVS, and SmartReflex

[2] Measured value; Device is off except for wakeup domain, wakeup domain external supply voltage = 1.8V; VDD1, VDD2, VDDS_DPLL_DLL, VDDS_DPLL_PER, all 0V and disabled (for power savings in external regulators); power consumed is I/O leakage (this is application board dependent) and wakeup domain leakage; room temp.; limited ES2.1 sample size, might not reflect worst case silicon.

[3] Measured value; VDD1 = 0.9V, VDD2 =0.9V; wakeup domain external supply voltage = 1.8V, VDDS_DPLL_DLL, VDDS_DPLL_PER at their normal operating values; room temp.; limited ES2.1 sample size, might not reflect worst case silicon.

[4] Measured value; Power consumed on VDD1 (processor supply rail) and measured with MPU running Dhrystone 2.1 infinite loop; room temp; ES2.1 nominal unit, SmartReflex not used.

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•These are preliminary power estimates for OMAP35x only based on full utilization of power reductions techniques for active use cases (MP3 decode, MPEG4 decode)

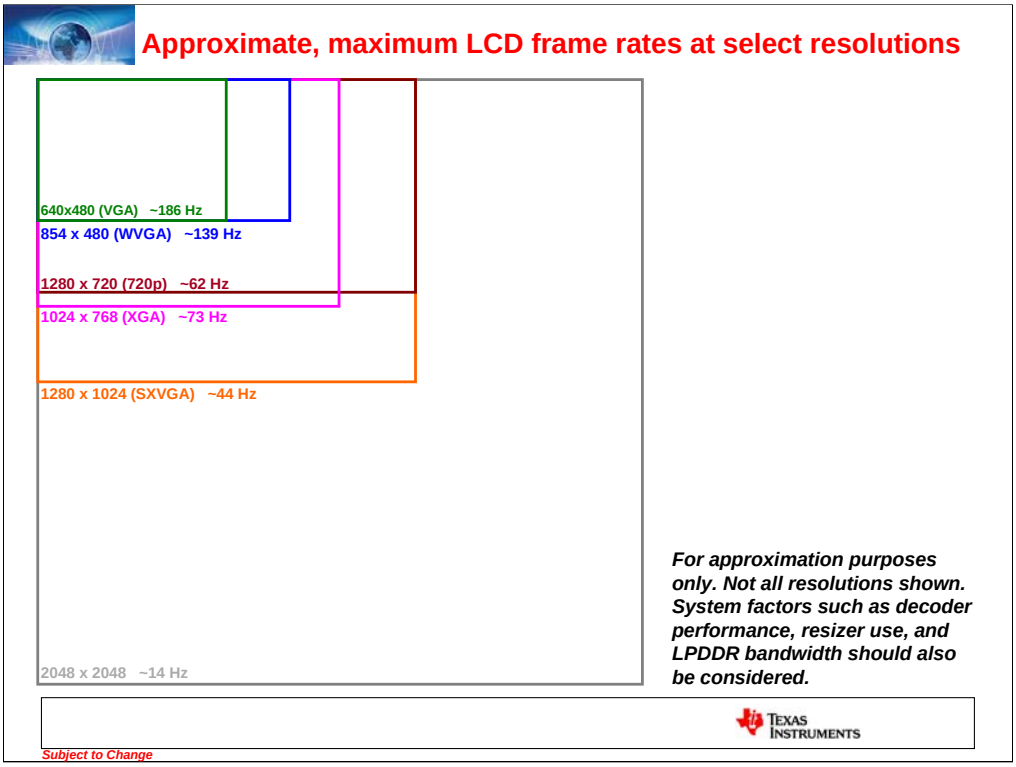
•They are full chip estimates with the exception of ARM cortex-A8 only mA/mHz/V, which is for the processor only

•Generally TI is conservative on quoting power numbers for example:

- •We have MP3 decode estimates as low as 16 mW
- •We have MPEG4 SP D1 decode estimates as low as 220mW

OMAP35x display subsystem maximum resolution

- LCD Output
  - LCD output can support a maximum display resolution up to 2048 x 2048 with the pixel clock limited to 74.25 MHz.
  - However, the display resolution and pixel clock will limit the maximum frame rate that can be supported. Keep in mind that the display area must also account for blanking fields which are specified by the standard being used, i.e. VESA, CEA-861-D, etc.
  - An approximation for the maximum frame rate can be obtained by: *approx max frame rate = (74250000 / (X * Y * 1.3))*, where the 1.3 factor is related to blanking times.
    - For direct drive LCD's the 1.3 can be replaced with a value closer to 1.
    - This is an approximation only. Care should be taken to do a more thorough analysis before a final decision is made.
- TV Output
  - TV output is always NTSC or PAL standard definition.

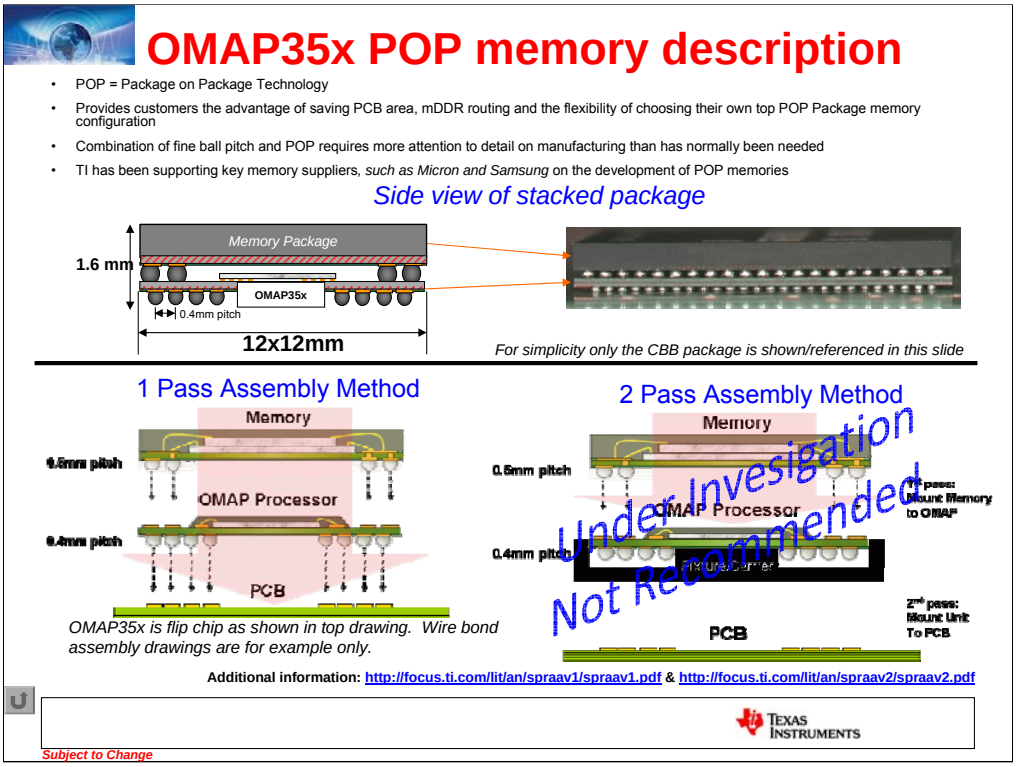


•OMAP35x LCD controller can support up to 2048 x 2048. However, the challenge is normally keeping enough data flowing to support this resolution.

•Maximum pixel resolution of OMAP35x LCD controller is 2048 x 2048 with clock limited to 74.25 MHz

•General rule of thumb for the maximum frame rate (74250000 / (X * Y * 1.3)).

- •For direct drive LCD's the 1.3 can be replaced with a value closer to 1 (this factor is related to blanking times on LCD's)
- •This is an approximation only. Care should be taken to do a more thorough analysis before a final decision is made.



•POP is new to many PCB manufactures although POP technology is not inherently new. The combination of POP and fine ball pitch requires greater attention to detail than has normally been required. Extra time will be needed to work through challenges as manufacturing houses come up-to-speed. Bringing up pop technology in conjunction with small ball pitch requires close communication with board shop, memory vendor, TI, and customer.

- •Moving ahead with POP should not be trivialized by the customer. This is an investment the customer will have to make to enjoy the many benefits.
- •Once scenario is understood and the learning curve surpassed manufacturing can yield reasonably high yield rates.
- •Before starting a design based on POP memory customers should speak with their TI representative.

•The main challenges with POP is not POP in and of itself. It is what the POP package does to OMAP as it cools. The memory balls solidify in the cool down process before the OMAP does which causes the balls on OMAP to be pulled away from the PCB. The soldering issues are between OMAP and the PCB. As the heat comes down from the top, the memory is heated first and cools first. That is where the issues are. Too much solder on the OMAP causes shorts, which cannot be fixed. Not enough causes opens.

•Pre-assembled POP + memory assemblies are not available. Customers must procure their own memory and OMAP devices.

•2 pass assembly method is not recommended at this time due to reliability issues

OMAP35x extended temperature and reliability information

To avoid significant device degradation for commercial temperature OMAP35x devices (0°C ≤ Tj ≤ 90°C), the device power-on hours (POH) must be limited to one of the following:

- 100K total POH when operating across all OPPs and keeping the time spent *at* OPP5 to less than 23K POH.
- 50K total POH when operating *exclusively* at OPP5.
- 44K total POH with *no restrictions* to the proportion of these POH at operating points OPP1 - OPP5.

To avoid significant device degradation for industrial temperature OMAP35xA devices (-40°C ≤ Tj ≤ 105°C), the following restrictions apply:

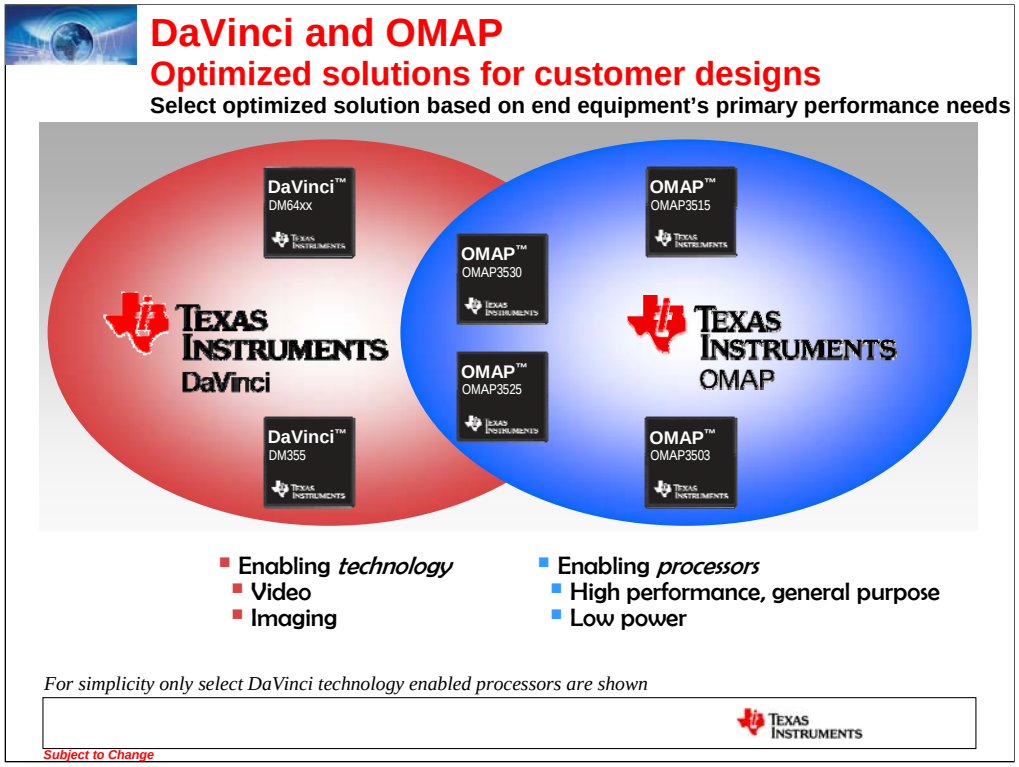
- OPP5 is not supported.*
- The total device POH must be limited to less than 50K.*

*If an industrial temperature device is operated such that Tj never exceeds 90C (-40°C ≤ Tj ≤ 90°C) then the OPP POH limits for commercial devices indicated above apply.

Note: Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Tj = junction temperature

OPP = Operating Performance Point



•DaVinci technology is a video enabling technology based around 4 pillars

- Software, Support, Ecosystem,Silicon

•DaVinci is intended to make video and imaging easy

•OMAP is very focused around enabling processors. OMAP is often categorized by high performance, general purpose, for example the Cortex A8, and low power

•These are not hard and fast definitions only general guidelines

•Some examples of DaVinci technology based solutions are DM64xx and DM355

•OMAP3503 and OMAP3515 are examples of OMAP technology

•OMAP3530 and OMAP3525 will be branded as "OMAP featuring DaVinci technology".

- These devices are good examples of where the brands will overlap

Potential OMAP35x applications

Digital Signage

Point of Service Terminals

Low Power PC / Web Tablet

Portable Industrial / SDR

Portable Infotainment

Industrial Panel PC/HMI

TEXAS INSTRUMENTS

Subject to Change

Difference between OMAP35x and OMAP59x

Some customers had unsatisfactory OMAP59x experiences because:

- The most robust application support was limited to PDAs
- All support required third party involvement
- There was no standard software framework to simplify system integration
- This was TI's first attempt to promote dual core SOC's (ARM + DSP + peripherals) to the mass market

Customers will have more success with OMAP35x because:

- TI is delivering tools enabling a broad array of applications to use OMAP35x thus third party support is optional, not required
- TI is porting the DaVinci technology framework to OMAP35x to simplify system integration
- TI has proven robust broad market support of complex SOCs with success of DaVinci technology based DM644x
- There has been more collaboration between TI business units on the general OMAP 3 technology
- There is more TI technical staff supporting OMAP35x

Texas Instruments

Subject to Change

OMAP™ 3 based hardware solutions

	TI OMAP35x EVM	LogicPD OMAP35x Dev. Kit / Medical EVM	Beagle Board (OMAP35x)	LogicPD Zoom Mobile Development Kit (OMAP34x)	OMAP34x SDP
Part Number	TMDXEVM3503	TMDSMEVM3503-L	TBD	LDP3430-VG1.0.0	--
Approximate Relative Pricing	10x	7x	1x	6x	33x
Support Channel	TI PIC	Distribution & www.logicpd.com	Community	Distribution & www.logicpd.com	--
Availability	Now	Now	August 2008 via Digi-Key	Now	Now
Customer Target	Targeted for broad market	Limited design resources Time to Market Pressures Looking for an off the shelf product-ready solution	Hobbyist, "Hackers", University students	High volume mobile phone developers	High volume mobile phone developers
Applications Target	All applications suitable for OMAP	Embedded System applications such as Medical, Industrial, gaming, POS, etc.	Software development only	Mobile / Cellular Phones	Mobile / Cellular Phones
Weblink:	Link	Link	Link	Link	Link
Notes		General TI FAE's and factory applications will not have this board TI OMAP35x EVM software not tested on this board	General TI FAE's and factory applications will not have this board TI OMAP35x EVM software not tested on this board	General TI FAE's and factory applications will not have this board TI OMAP35x EVM software not tested on this board	General TI FAE's and factory applications will not have this board TI OMAP35x EVM software not tested on this board

Texas Instruments

Subject to Change

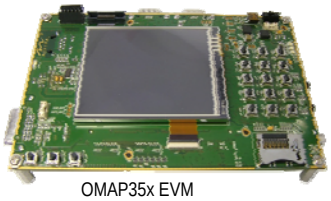
•There are several OMAP 3 technology based boards that are in or have been in the market.

•Each board was designed and intended to meet a unique portion of the overall market as such each board has specific limitations with regard to availability and support

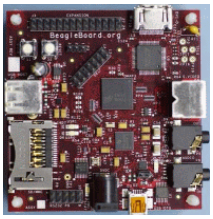
•The main board our customers should focus on is the OMAP35x EVM. This the board that TI FAE's and factory apps will have to work with. The other boards will be limited to those engineers actively involved in those projects.

•Individual 3P's may have their own boards as well.

OMAP™ 3 based hardware solutions

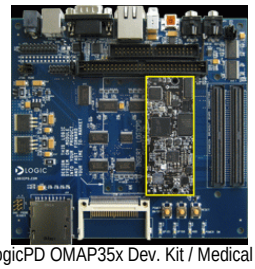


OMAP35x EVM
4.25" x 7"



Beagle Board
3" x 3"

OMAP34x SDP
8.5" x 11"



LogicPD OMAP35x Dev. Kit / Medical EVM
5.75" x 6.25"

LogicPD OMAP34x Mobile Development Kit
3.8" x 6.3" x .95"

Not to scale. Approximate size noted (in inches)

Texas Instruments

Subject to Change

Zoom OMAP35x medical & general purpose development kit

- Out of the box and into development – *Quickly*
  - TI & Logic orderable part #: **TMDXMEVM3503-L**
  - Suggested resale price: $995
  - Shipping now
- Platform details
  - Includes OMAP35x System On Module (SOM)
  - 4.3" WQVGA Sharp LCD with integrated touch
  - Ethernet RJ-45, DB9 & USB-B UART, USB Type-A & Mini-AB
  - SD/MMC card slot
  - Audio in/out connectors
  - Compact Flash card slot
  - High density expansion breakout board
  - **TI High Precision Analog adapter board**
  - Debug LEDs and buttons
  - 2.4Ghz whip antenna and RF cable
  - USB, Ethernet, and UART cables included
  - International power supply (US, Japan, Europe)
- Available software
  - Windows CE 6.0 BSP
  - Open source Linux BSP, kernel 2.6.22
  - Green Hills Integrity BSP (Provided by GHS)
  - **More to come…**
- Design files
  - BOM, PDF of schematics and layout for SOM
  - Full design files for the carrier board

Zoom Development Kit
(shown with optional 6.4" VGA Display Kit)

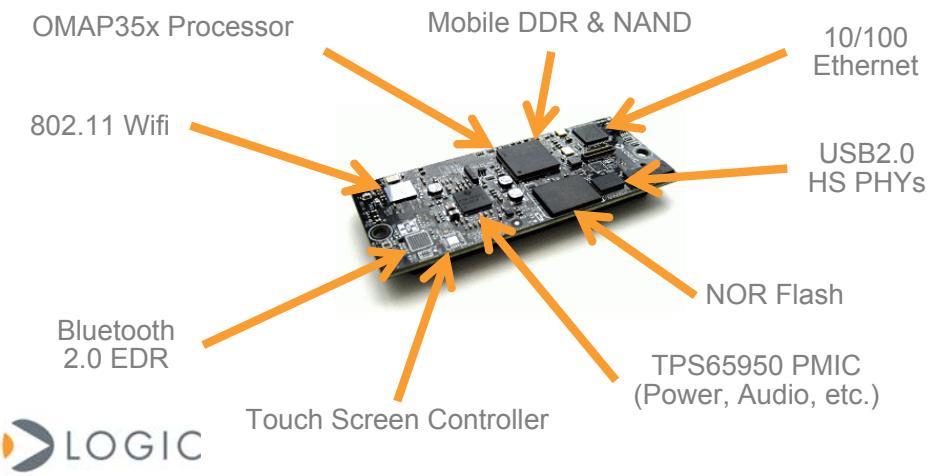
Additional information: http://www.logicpd.com/products/devkit/ti/zoom_omap3_development_kit

Texas Instruments

Subject to Change

What is a System On Module?

A pre-built production ready module that incorporates the HW and SW required in new medical and other products.



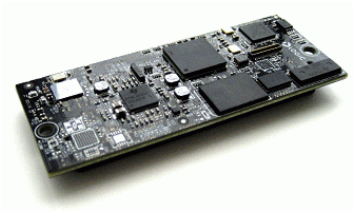
LOGIC

Texas Instruments

Subject to Change

OMAP™ 3 SOM-LV System On Module

- Production-ready – *Integrate into end-products with ease*
  - Logic part #: **SOMOMAP3530-10-1670EFCR-A**
  - 128MB mDDR, 256MB NAND, Audio, Touch
  - Logic part #: **SOMOMAP3530-10-1672IFCR-A**
  - 128MB mDDR, 256MB NAND, Audio, Touch, 8MB NOR, 10/100 Ethernet, 802.11 B/G, Bluetooth
- SOM-LV Type III
  - Extremely small form-factor! (31 x 76 x 7.4mm)
  - Industrial temperature option: -40 C to 85 C
  - Committed to 10+ year product offering
- Features
  - Supports all OMAP3x SKUs (3430, 3503 3515, 3525, 3530)
  - Mobile DDR SDRAM memory 128 or 256MB
  - NAND & NOR flash memory 128 or 256MB
  - **LCD controller can drive XGA displays!**
  - 10/100 Ethernet
  - 3x UART, SPI, I2C, SSI, McBSPs
  - 2x High Speed USB (1 OTG and 1 Host)
  - 802.11 B/G (CSR chipset)
  - Bluetooth 2.0 +EDR (TI chipset)
  - 4-wire touch screen controller
  - 2x SD/MMC and Memory Mode Compact flash support



LOGIC

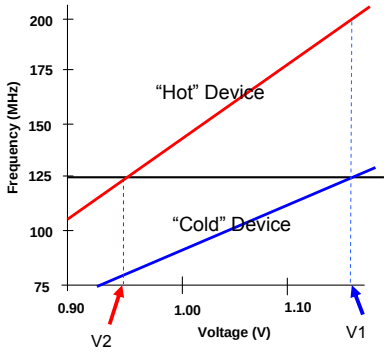
Additional information: http://www.logicpd.com/products/devkit/ti/zoom_omap3_development_kit

Texas Instruments

Subject to Change

SmartReflex™ adaptive voltage scaling

- Silicon manufacturing process yields a distribution of performance capability
- For a given frequency requirement:
  - Devices on hot/strong/fast end of distribution can meet this at a lower voltage
  - Devices on cold/weak/slow end of distribution need higher voltage
- Simple system will set the higher voltage (V1) for operating all devices based on the cold devices requirements
- Smarter system will adapt operating voltage per device (V1, V2, …)



Red line: Hot device (faster but higher power)
Blue line: Cold device (slower but lower power)

OMAP35x: NEON™ or C64x+™ DSP w/ accelerators a simplistic view

	NEON	C64x+ w/ accelerators
What it is	Enhanced instructions inherent to ARM Cortex A8	Standalone, independent DSP engine
Major Benefits	Integration into the Cortex A8 allows for simplified software systems and some DSP functions on Cortex A8	Truly separate processing core enabling highest performance DSP functions, including video and multimedia, while leaving the Cortex A8 free to process other items such as GUI, connectivity, etc.
Notes	Multimedia codec development entirely via ecosystem partners	TI's primary focus for enabling multimedia codecs

Additional information: http://www.arm.com/products/CPUs/NEON.html
Additional information: http://focus.ti.com/lit/ug/sprufa3a/sprufa3a.pdf

Texas Instruments

Subject to Change

If additional information link does not work for TI, please use this one: http://focus.ti.com/docs/prod/folders/print/omap3530.html#technicaldocuments and select the IVA2.2 doc

OMAP35x EVM schematics, Gerber files, and symbols

OMAP35x EVM schematics are included as part of the documentation which comes with the EVM

- They are also available in PDF on the EVM update site as part of the release package (available to registered EVM users)
- Schematics, gerbers, and assembly drawings are also available in PDF from Mistral's OMAP35x EVM support site (short, free registration process required)
  http://www.mistralsolutions.com/assets/downloads/3530.php

Non PDF versions of schematics and gerbers should be requested directly from Mistral via support@mistralsolutions.com

Orcad symbols and Allegro footprints can be found at:

http://www.ti.com/OMAP3530 (look under "more literature")

Micron POP memory devices

Micron MCP Datasheet Access

All Micron MCP datasheets will be available online through the secure site.

The following steps will assist you in reaching the Secure Micron product pages that contain the product information for which you are searching.

1. Go to www.micron.com. You will find on the right side of the blue bar that runs across the page a link that says "Login" if you are not already logged in to your Micron.com account. Click this link and login.

   Note: If you are already logged in, the link will display your name and the word "Account." For example: "Roger's Account" Click this link.

2. If you do not already have a Micron account, you will see a link on the Login page that allows you to request an account.
3. Once logged in (https://www.micron.com/my/), you will see a link titled "Secure Products Site". Click this link.
4. This link will allow you to see the secure sections to which the product group had previously granted you access (there may be more than one). Click on the link of your choice.
5. On the next page, you will see a list of documents. Click on the document link of your choice to view and download the document.

Please note that to download a datasheet, you will be requested to approve an online NDA form that covers only the datasheet being downloaded. All further documentation and design discussions will need to be covered under a general NDA with Micron.

- **Micron MCP Datasheet Directories**
- 160b_15x15_JEDEC_PoP
- 152b_14x14_OMAP_PoP
- 152b_14x14_JEDEC_PoP
- 168b_12x12_OMAP_PoP
- 128b_12x12_JEDEC_PoP
- 107b_10.5x13.0mm_JEDEC_MCP
- 137b_10.5x13.0mm_JEDEC_MCP
- 149b_10.0x13.5mm_JEDEC_MCP
- 199b_12.0x18.0mm_JEDEC_MCP

- To request access to a directory listed above, email mcpsupport@micron.com after you have established your micron.com account.

•This slides describes the procedure for accessing Micron POP package memory information. It also includes the directories / groups of POP options from Micron for OMAP35x

OMAP™ 3 multimedia stacks for OMAP34xx and OMAP35x

- TI has plans to offer two methods for launching multimedia algorithms on OMAP 3 platforms
- OMAP34xx
  - Customers will be provided with an implementation of the Khronos Group OpenMAXTM IL ("Integration Layer") standard
    - OpenMAX IL is a cross-platform API that provides comprehensive streaming media codec support and application portability
  - DSP Bridge is a supporting software driver for the OMAP34xx OpenMAX IL library that is developed to meet the DSP-accelerated multimedia requirements of mobile handset customers
  - Focuses on mobile / cellular customers
- OMAP35x
  - Multimedia support will be provided via Codec Engine with DSP/BIOS Link
  - These components provide for fully utilizing the DSP to accelerate codecs and to execute other DSP algorithms, not necessarily intended for multimedia
  - Codec Engine provides the ease-of-use of a single-threaded programming model
  - Targeted for broad market, tested and ported on the OMAP35x EVM
- For the future, compatible and enhanced versions of both Codec Engine and DSP/BIOS Link will be provided as the supporting software driver layer for an OpenMAX IL library

Texas Instruments

Subject to Change

OMAP35x ES3.0 planned updates, fixes, and schedule

Specification changes summary

- Support for decoupling FS/LS & ULPI TLL/PHY interfaces
  - Compatible with ES2.x if port1 only is used. If other port than port1 is used then the bit value written in UHH_HOSTCONFIG[0] should be replicated in UHH_HOSTCONFIG[11] and UHH_HOSTCONFIG[12] on ES3.0 to ensure same behavior as ES2.x.
- Programmable polarity of USB TxEN
  - Compatible with ES2.x
- DSS support to HDMI
  - Compatible with ES2.x
- Change Revision number: IDCODE
  - Software compatibility: Not Relevant
- USB descriptor left blank
  - Compatible with ES2.x

Errata fixed summary

- DSS dependency with CORE-L3 missed
  - Compatible with ES2.x
- Peripheral boot issue when using external crystal
  - Compatible with ES2.x
- Dummy data sent when enabling the video mode
  - Compatible with ES2.x
- Context restore failure on GP devices if OCM RAM is OFF after wake-up
  - Compatible with ES2.x

Schedule

- Errata update late July ‘08
- Samples September ’08
- TMS / production 4Q’08 - CUS and CBB packages; 1Q’09 CBC package

ES 2.1 will not be TMS / qualified

Texas Instruments

Subject to Change

Device comparison

OMAP35x/DM644x/DM643x/DM3xx – comparison

Core Feature	OMAP3530/25	OMAP3503/15	DM6446	DM6443	DM6437/5/3	DM35x
CPU	ARM Cortex A8	ARM Cortex A8	ARM926EJ/C64x+	ARM926EJ/C64x+	C64x+	ARM926EJ-S
CPU Frequency	Up to 600 MHz	Up to 600MHz	297/594MHz	297/594MHz	400-600MHz	216-270MHz
Float support	Neon	Neon	No	No	No	No
Core Internal Instruction Memory	16KB cache	16KB cache	ARM: 16KB cache/ 8KB RAM; DSP: 32KB cache/SRAM	ARM: 16KB cache/8KB RAM; DSP:32KB cache/RAM	32KB cache/SRAM	16KB cache
Core Internal Data Memory	16KB cache	16KB cache	ARM:16KB cache; DSP:80KB cache/RAM	ARM:16KB cache; DSP:80KB cache/RAM	80KB cache/RAM	8KB cache
L2 Memory	256KB	256KB	64KB	64KB	128KB	0KB
Embedded SRAM	None	None	None	None	None	32KB
Multiply Accumulate Capability	ARM MAC, IVA Subsystem (C64x DSP 360-430MHz)	ARM MAC	ARM MAC and C64x+ DSP 400-594MHz at 3200-4752MMACs	ARM MAC and C64x+ DSP 400-594MHz at 3200-4752MMACs	3200-4800MMACs	ARM MAC
Video Capabilities	MPEG4 720P 24fps/30fps Encode/Decode H.264 MP VGA Decode H.264BP/VC1/ WMV9 D1 Encode/Decode	MPEG4 D1 24fps/30fps Encode/Decode H.264 BP D1 12fps/30fps Encode/ Decode	DSP MPEG4 SP 30fps 720P/D1 Decode/Encode WMV9/VC1 30 fps 720P/D1 Decode/Encode H.264 BP 30fps D1 Decode/Encode H.264 MP D1 30fps Decode	MPEG4 SP 720P 30fps Decode WMV9/VC1 720P 30 fps Decode H.264 BP D1 30fps Decode H.264 MP D1 30fps Decode	MPEG4 SP 30fps /D1 Decode or Encode half duplex; full duplex at VGA WMV9/VC1 30 fps D1 Decode H.264 BP 30fps D1 Decode/ VGA Encode at half duplex; full duplex at CIF H.264 MP D1 30fps Decode	MPEG4 SXVGA 30fps Encode and Decode JPEG 75MPixels-per-sec Encode and Decode

Texas Instruments

Subject to Change

OMAP35x/DM644x/DM643x/DM3xx – comparison cont'd

Core Feature	OMAP3530/25	OMAP3503/15	DM6446	DM6443	DM6437/5/3	DM35x
Video performance	Programmable DSP	Programmable ARM Cortex A8	Programmable DSP	Programmable DSP	Programmable DSP	HW accelerator
Image Pre/Post Processing	Color space convert, white balance, resize, histogram, auto focus	Color space convert, white balance, resize, histogram, auto focus	Color space convert, white balance, resize, histogram, auto focus	Resize	Color space convert, white balance, resize, histogram, auto focus (DM6437/5) Resize only (DM6433)	Color space convert, white balance, resize, histogram, auto focus
2D/3D Graphics	2D/3D graphics accelerator- IMG SGX530 (OMAP3530 only)	2D/3D graphics accelerator- IMG SGX530 (OMAP 3515 only)	No	No	No	No
LCD Controller Display Size	Up to 1080i/720p digital NTSC/PAL analog	Up to 1080i/720p digital NTSC/PAL analog	Up to 1080i/720p digital NTSC/PAL analog	Up to 1080i/720p digital NTSC/PAL analog	Up to 1080i/720p digital NTSC/PAL analog (DM6437,DM6433)	Up to 1080i/720p digital NTSC/PAL analog
Camera Interface	CCIR656, 16-bit parallel YCC/RGB	CCIR656, 16-bit parallel YCC/RGB	CCIR656, 16-bit parallel YCC/RGB	No	CCIR656, 16-bit parallel YCC/RGB (DM6437,DM6435)	CCIR656, 16-bit parallel YCC/RGB
Flash Boot	NAND, NOR, MMC/SD	NAND, NOR, MMC/SD	NAND, NOR	NAND, NOR	NAND, NOR	NAND, NOR, MMC/SD
DDR	DDR@166MHz	DDR@166MHz	DDR2@166MHz	DDR2@166MHz	DDR2@166MHz	DDR@ 171MHz
DMA channels	32	32	64	64	64	64
SSI/i2S	1 SSI, 5 McBSP	1 SSI, 5 McBSP	1 ASP	1 ASP	1 McASP	2 McBSP
RTC	No	No	No	No	No	No
UART	2-3	2-3	3	3	2	3

Texas Instruments

Subject to Change

OMAP35x/DM644x/DM643x/DM3xx – comparison cont'd

Peripheral Feature	OMAP3530/25	OMAP3503/15	DM6446	DM6443	DM6437/5/3	DM35x
Timers	12	12	2	2	2	6
I2C	4	4	1	1	1	1
IrDA	Serial Infrared, Medium Infrared, Fast Infrared	Serial Infrared, Medium Infrared, Fast Infrared	No	No	No	No (external)
Configurable SPI	4	4	2	2	1	3 (2 chip selects each)
Single Wire Interface	Yes	Yes	No	No	No	No
Memory Stick Controller	Yes	Yes	Yes	Yes	No	Yes
Watch Dog Timer	Yes	Yes	Yes	Yes	Yes	Yes
PWM	No	No	3	3	3	4 (+4 RTO)
MMC/SD	3	3	1	1	No	2
PCMCIA/ Compact Flash	Through EMIF	Through EMIF	Through EMIF	Through EMIF	Through EMIF	Through EMIF
Smart Card Interface	No	No	No	No	No	No
HDD Interface	Through EMIF	Through EMIF	ATA6	ATA6	Through EMIF	Through EMIF
WiFi support	Host interface through SDIO, CF or USB	Host interface through SDIO, CF or USB	Host interface through SDIO, CF or USB	Host interface through SDIO, CF or USB	Host interface through VLYNQ	Host interface through SDIO
USB	1 HS OTG and 3 Host	1 HS OTG and 3 Host	1 HS and 1 HS/FS Host	1 HS and 1 HS/FS Host	No	1 HS/FS and 1 HS/FS Host Integrated USB2.0 Phy HS OTG (DM355 only)

Texas Instruments

Subject to Change

OMAP35x/DM644x/DM643x/DM3xx – comparison cont'd

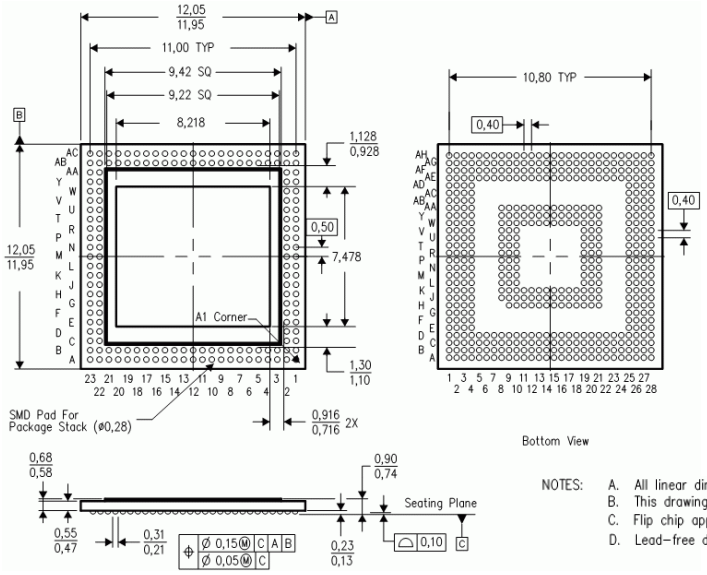
System Feature	OMAP3530/25	OMAP3503/15	DM6446	DM6443	DM6437/5/3	DM35x
EMAC	No	No	10/100	10/100	10/100	No
Security	HW accelerator	HW accelerator	No	No	No	No
Package Pin #/Type/ Size in mm	12x12mm POP 0.4mm spacing; 16x16mm Non-POP; 0.65mm spacing 14x14mm POP 0.5mm spacing	12x12mm POP 0.4mm spacing; 16x16mm Non-POP; 0.65mm spacing 14x14mm POP 0.5mm spacing	361 pin BGA 16x16 0.8mm spacing	361 pin BGA 16x16 0.8mm spacing	361 pin BGA 16x16 0.8mm spacing 23x23 mm 1.0 mm spacing	329 PBGA 12x12 0.5mm (DM350) 337 PBGA 13x13 0.65mm (DM355
Power Management	DVFS (0.9-1.35V) Standby 0.9V 10 power domains Smart Reflex AVS (adjust for process/temp)	DVFS (0.9-1.35V) Standby 0.9V 10 power domains Smart Reflex AVS (adjust for process/temp)	None	None	None	None
Process	65nm	65nm	90nm	90nm	90nm	90nm
Availability (TMX/TMS)	Now for 0.4mm & 0.65mm spacing/TMS 4Q08 Sep. 08 for 0.5mm spacing / TMS 1Q09	Now for 0.4mm & 0.65mm spacing/TMS 4Q08 Sep. 08 for 0.5mm spacing / TMS 1Q09	Now	Now	Now	Now

Texas Instruments

Subject to Change

OMAP35x package drawings

CBB – 12 x 12 mm, 0.4mm pitch, POP

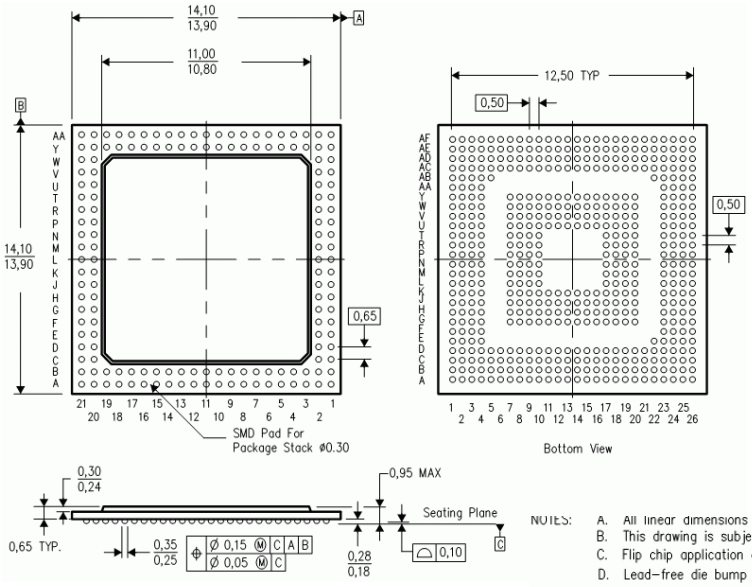


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Lead–free die bump and solder ball.

TEXAS INSTRUMENTS

Subject to Change

CBC – 14 x 14 mm, 0.5mm pitch, POP



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Lead–free die bump and solder ball.

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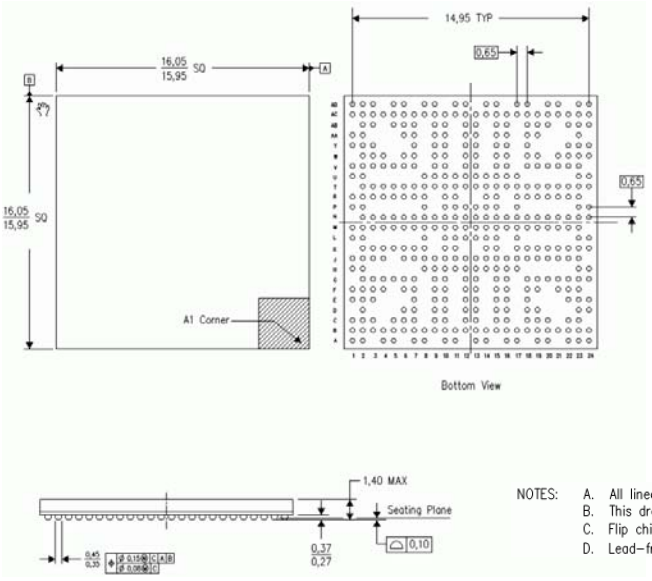
CUS – 16 x 16 mm, 0.65mm pitch, Via Channel™ array



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Lead–free die bump and solder ball.

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Subject to Change