MSP430F5xx Generation Architecture Overview & the MSP430F5438

WW MSP430 Applications

Texas Instruments

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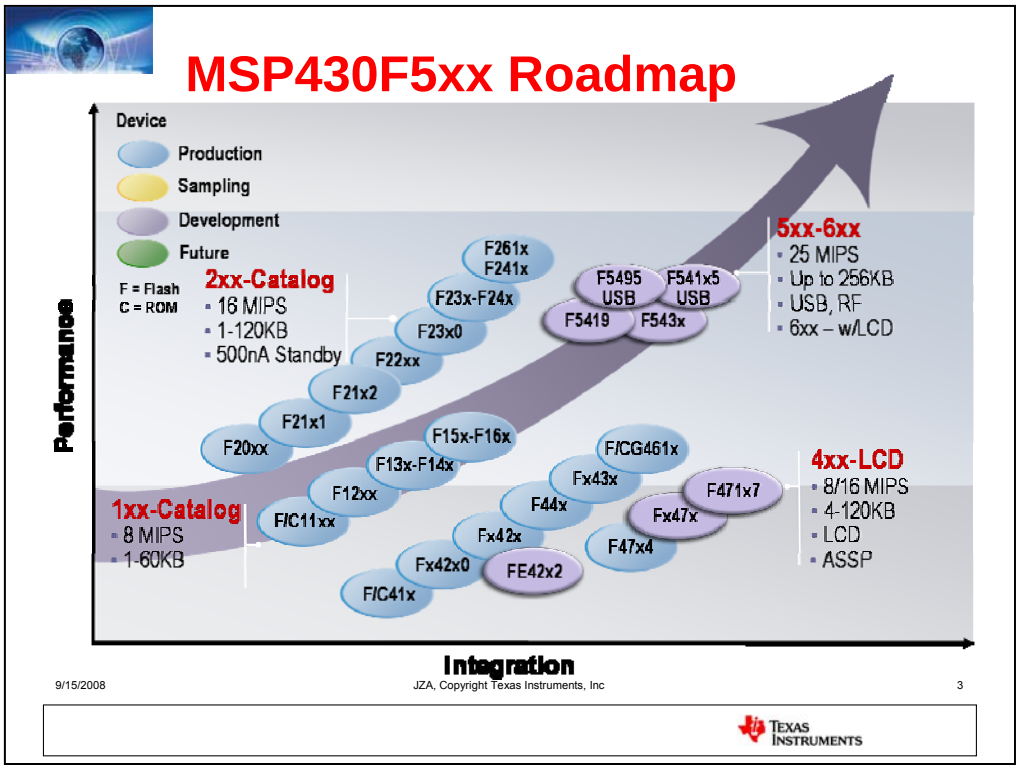
Agenda

- ‘5xx Overview
- ‘5xx/’F54xx Core Architecture
- ‘5xx/’F54xx Enhancements
- Tools support



The MSP430 is world's most popular low-power MCU architecture with 100 compatible devices in production today.

The **MSP430x1xx** family was introduced in 2000 to address requirements for catalog low-power MCU applications. The F1xx family spans from the entry-level C1101 ROM device starting at $0.49, to highly integrated F16xx devices with up to 60kB of Flash / 10K RAM, 12-bit ADC, 12-bit DAC and a DMA controller. The F1xx family introduced the world's ultra-low power Flash and is specified for operation at up to 8-MIPS from 1.8V to 3.6V. All F1xx family members are in high-volume production. Existing F1xx devices are encouraged for new designs, though no new F1xx devices are planned. Future catalog MSP430's will be developed in the F2xx family.

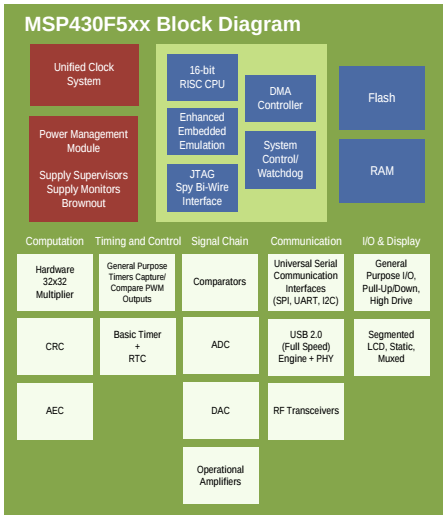
The **MSP430F4xx** offers application specific standard products (ASSP) solutions targeted to metering and measurement equipments. The F4xx complements the F1xx family adding an LCD driver, zero power BOR on all devices and an enhanced Frequency Locked Loop (FLL) clock system. The F4xx family has the same operating characteristics as the F1xx including ultra-low power Flash operation at up to 8-MIPS from 1.8V to 3.6V. The F4xx offers a high-resolution 16-bit sigma-delta A-D converter, operational amplifiers, and other mixed-signal intelligent peripherals ideal for single-chip metering and measurement applications. Additional F4xx derivatives are planned and the family is encouraged for new designs.

The **MSP430F2xx** family provides twice the processing performance at half the stand-by power consumption compared to MSP430F1xx devices. The F2xx family offers enhancements that reduce overall system cost and improve reliability making these new devices an ideal roadmap solution for existing low power F1xx designs or as a launch point for new applications. The F2xx family began introduction in 2005 and will continue for the next several years.

The **MSP430x5xx** is released for sampling June 9 2008 and will be available in late 2008. The F5xx family will be fully compatible with existing MSP430's offering expanded memory, more speed and a variety of new peripherals including USB and RF in 2009-2010.

5xx Architectural Advances

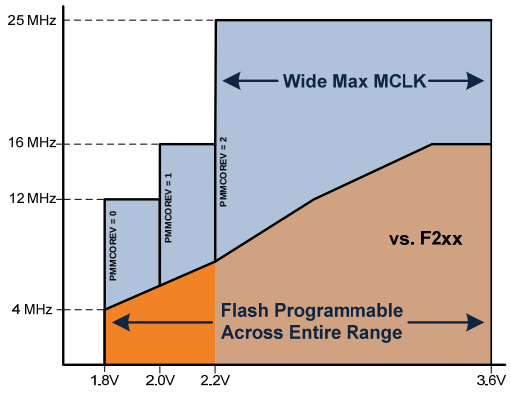
- **Ultra-Low Power**
  - 160 µA/MIPS
  - 2.5 µA standby mode
  - Integrated LDO, BOR, WDT+, RTC
  - 12 MHz @ 1.8V
  - Wake up from standby in <5 µs
- **Increased Performance**
  - Up to 25 MHz
  - 1.8V ISP Flash erase and write
  - Fail-safe, flexible clocking system
  - User-defined Bootstrap Loader
  - Up to 1MB linear memory addressing
- **Innovative Features**
  - Multi-channel DMA supports data movement in standby mode
  - Industry leading code density
  - More design options including USB, RF, encryption, LCD interface



The MSP430F5xx is the next generation technology platform for the MSP430 family and continues to expand on MSP430's industry leadership in the ultra-low-power 16-bit MCU space. The 5xx family offers improved ultra-low-power performance with innovative new power conserving features such as adjustable core voltage and an integrated low-power LDO. Cutting edge power efficiency is available through an innovative power management system as well as record breaking performance at 160 µA/MIPS with 256-KB flash and 16-KB RAM. The 5xx also offers increased peripheral performance, significantly higher levels of integration and many new features designed for customer ease of use, all while remaining completely compatible with existing MSP430 families.

MSP430F5xx Operating Range

- 25MHz peak performance
- More performance across V_{CC} range
  - Flash ISP @ min. V_{CC}
  - 12MHz @ min. V_{CC}
  - Up to 25MHz @ 2.2V-3.6V
- Programmable V_{CORE} maximizes power efficiency
- Lowering V_{CC} or V_{CORE} reduces system current



This slide highlights the Vcc vs. CPU freq relationship of the 5xx family as compared to the existing 2xx. All MSP430 devices, including the F5xx operate in the wide range of 1.8 to 3.6V. Fundamental improvements were made to the F5xx including Flash programming at the minimum Vcc of 1.8V, increased CPU clock at both the upper and lower Vcc ends & a widened max CPU clock range of 25MHz at 2.2 – 3.6v. 12 MHz operation is possible even at the lowest Vcc of 1.8V.

Compared to the F2xx, where only 4MHz operation is possible at the min Vcc of 1.8v and the min Flash programming voltage was 2.2V (vs. 2.7V on the 4xx). On the 2xx, full speed 16MHz operation is only possible at 3.3v or higher.

Also shown is the core voltage programmability that the regulator in the PMM has enabled. This provides the user the ability to optimize the Vcore level to the performance needed by the given application for maximum power efficiency.

What Has Changed?

1xx	2xx	4xx	5xx
Basic Clock System	Basic Clock System +	FLL, FLL +	Unified Clock System UCS
Core voltage same as supply voltage	Core voltage same as supply voltage	Core voltage same as supply voltage	Programmable Core Voltage with integrated PMM
16-bit CPU	16-bit CPU, CPUX	16-bit CPU, CPUX	16-bit CPUXV2
GPIO	GPIO w/ pull-up and pull-down	GPIO	GPIO w/pull-up and pull-down, drive strength
N/A	N/A	N/A	CRC16
Software RTC	Software RTC	Software RTC with Basic Timer, Basic Timer + RTC	True 32-bit RTC w/Alarms
USART	USCI, USI	USART, USCI	USCI, USB
DMA up to 3-ch	DMA up to 3-ch	DMA up to 3-ch	DMA up to 8-ch
MPY16	MPY16	MPY16, MPY32	MPY32
ADC10,12	ADC10,12	ADC12	ADC12_A
4-wire JTAG	4-wire JTAG, some devices with Spy-Bi-Wire	4-wire JTAG	4-wire JTAG and Spy-Bi-Wire

So a lot has changed from the previous families as shown on this slide.

UCS – Compare this with the clock system of the past MSP430 devices. With this clock system you can pretty much connect any clock source to any of the clock nets driving the CPU and peripherals (MCLK, ACLK, SMCLK) with more FLL reference capability. A low power, low frequency oscillator has been added that has low accuracy and runs at 12KHz. Good for non-critical applications.

Power Management Module - Programmable core voltage conserves power when the CPU frequency can be reduced for the application. Keep in mind there are some external LDOs from TI that allow you to change the output voltage as well for the older devices without the PMM.

CPU – still a 16 bit core but no paging for the extended addressing. Core frequency is also increased.

The GPIO is more flexible/capable with the 5xx devices with pull-ups/downs and programmable drive strength. I/Os can be 16 bits wide when combined and also provide interrupt capability.

The CRC module has been added and is a separate module. This is a nice feature because it can be used with any peripheral. Compare this with some competing devices where the CRC is integrated with say the SPI module or something.

No more software overhead to wake up and perform the RTC function. The 5xx has this as a 32 bit counter. Can also be used as an interval timer.

USB will be added in future devices. This is new for the MSP430 family.

DMA channel capability has been increased. This is device dependent. Some have three for example.

MPY32 – 32 bit operands with a 64 bit result via 4 output registers. Retains backwards compatibility with the lower results registers.

ADC12_A – This is a much lower power ADC now (150uA instead of the 800uA from the 44x ADC). A big improvement is also the reference settling time. The old 44x reference stabilized in 17ms. The new reference is stable in 35us. A huge improvement.

‘F5xx vs. Prior MSP430 Generations

	2xx	4xx	5xx
CPU Clock (max)	16MHz	8MHz	25MHz
*Active Current (3.0V, typ)	515uA @ 1MHz 4.2mA @ 8MHz 9.1mA @ 16MHz	600uA @ 1MHz 4.8mA @ 8MHz N/A	220uA @ 1MHz 1.32mA @ 8MHz 3mA @ 16MHz
	120KB / 8KB (Flash / RAM)	120KB / 8KB (Flash / RAM)	256KB / 16KB (Flash / RAM)
Wake-up Time From LPM3	1us	6us	5us
Standby LPM3 Current	0.9 – 1.1uA	1.1 – 2.5uA	2.6uA (with active true RTC)
LPM4 Current	0.1uA	0.1uA	1.6uA (LPM4) / 0.1uA (LPM5)
Flash ISP Minimum DV_{CC}	2.2V	2.7V	1.8V
Port I/O Interrupt Capability	P1/P2	P1/P2	P1/P2 (F5438) Add’l pins in future devices
Prog. Port Pin Drive Strength	N/A	N/A	All port pins
Prog. Pull-ups/-downs	All port pins	N/A	All port pins
Available MCLK Sources	DCO LFXT1 XT2 (if available) VLO	FLL LFXT1 XT2 (if available)	UCS: FLL, LFXT1, XT2 (if available), VLO, REFO
Available FLL Reference Clocks	N/A	LFXT1	LFXT1, REFO, & XT2 (if present)

This slide tries to compare the devices that are the closest match to the 5xx device. The numbers kind of speak for themselves. The notes on the previous slide cover these topics as well.

Standby LPM3 Current – This number now has the active RTC included. In past devices you had to have a wake-up event and then perform the RTC function in software.

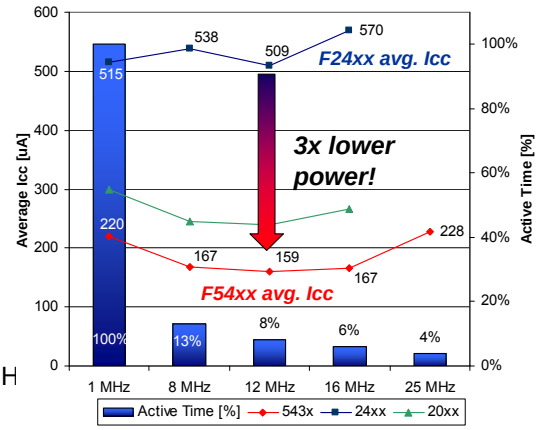
LPM4 Current – If you notice LPM4 is a little higher now than the older devices. We now have an regulator on chip that has an associated quiescent current. This requires additional current in LPM4, allowing full device functionality as expected with an MSP430: full RAM retention, fast wakeup on interrupts, etc. With that, note the new LPM5 mode. All other low power modes are the same as the previous families. LPM5 shuts down the regulator so everything is shut down. Exit/wakeup from LPM5 on the first 5xx devices is via reset.

Power numbers are for (typical):

F2418, F4618 & F5438

F543x: Real World Power Comparison

- Assume a generic real-world application:
  active + stand-by operation
- 1,000,000 clock cycle task every second (1 MIPS)
- ~3x lower power than F24xx (largest 2xx device)
- F5438 Advantages
  - 12MHz over Vcc: 1.8-3.6V
  - ~150uA/MHz @ 12MHz
  - <2mA active current @ 12MH
  - 2.6uA standby current



- Lower avg. power than F20xx, the smallest MSP430 device!
  - 256K vs. 2K Flash, 16K vs. 128B RAM

For a real world application, which spends most of it's time in standby mode and will wake up periodically to process a task, the F5438 will have the lowest average system power of any existing MSP430 ultra-low-power MCU.

For example, if we take a generic 1 MIPS task, meaning that it will required 1 million clock cycles worth of processing every second, the system only needs to be awake while its processing the task. So if the system running at 1MHz, it will be active 100% of time or if the system operates at 25MHz, it will be active only 4% of the time (1M/25M) and will be in standby mode the remaining 96% of the time.

If we compare the F5438 with F2418, the largest, comparable 2xx device, which is already ultra low power, the average current consumed is more than 3x lower on the F5438 than the F24xx across it's entire operating range. This is mainly due to the fact that the active mode current is significantly lower on the F5xx (150uA/MIPS @ 12MHz) than all existing MSP430 devices.

What's even more impressive, is that if we compare the F5438 to the smallest device in MSP430 portfolio with the lowest standby power, the F20xx, the average current on the F5xx is still about 30% lower! Considering that the F5438 has 128x more flash, 128x more flash and tons of other digital peripherals, this is great example of how the F5xx will drastically reduce the power consumption in most real world applications.

How does the F5xx achieve such low power consumption? At 12MHz, the devices consumes only 150uA/MIPS (<2mA) which is an industry leading number. Also, it can operate at 12MHz, a relatively high speed across the entire Vcc range. Operating at a lower Vcc will reduce power consumption. Despite it's high degree of integration it only consumes 2.6uA in standby mode.

NOTES:

F54xx, F24xx and F20xx current numbers taken from datasheet at 3v. The 16MHz data point is at 3.3v because the devices can't run at 3v at 16MHz. The F5438's 12MHz data point was measured on real hardware because the datasheet did not include this characterization yet.

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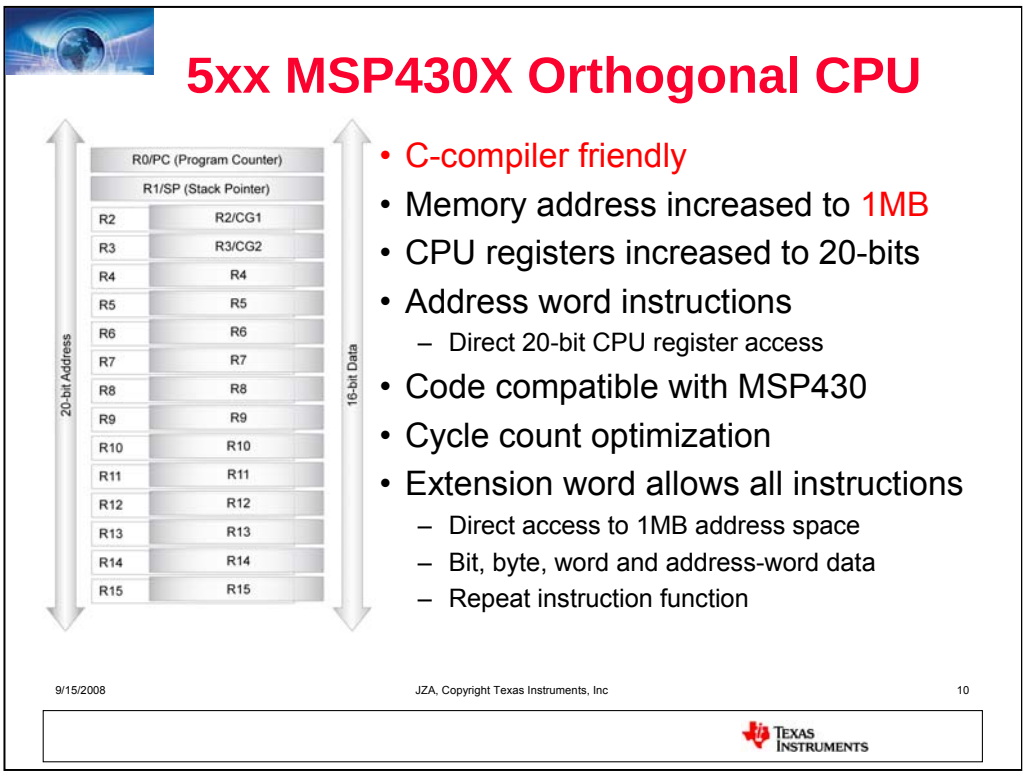


The new MSP430X architecture is 100% compatible with the MSP430 architecture and allows 16x more memory addressing page free using less code and fewer cycles.

The MSP430X is 100% compatible with the existing MSP430 allowing existing code libraries to be reused.

Extended addressing modes are incorporated that allow the existing MSP430 instruction set to operate page-free throughout the entire 1MB memory model with improved code density faster using fewer clock cycles. Extended instructions designed for the large memory allow optimal high-level code density with full backward compatibility, making it possible to develop very sophisticated real-time applications completely in modular C libraries.

The MSP430X executes MSP430 code unaltered in the compatible 64kB memory range. To further preserve compatibly, all MSP430X interrupt vectors, RAM and peripherals registers map exactly to the MSP430. The extended memory contains expanded code and data.

Existing MSP430 byte/word (.b/.w) addressing modes are expanded allowing direct access to 20-bit addresses (.a) fields which support 1MB (20-bit) program flow and pointer capability. This 20-bit address-word capability is accomplished for program flow, stack manipulation and pointer handling with same code density as the 16-bit MSP430 by using un-used bits in OP codes field. Additionally an extension word allows full 20-bit addressing for source and destination with any MSP430 instruction and addressing mode and added repetition capability.

Cycle counts have been reduced for several addressing modes and interrupt overhead allowing faster code execution.

Additional details regarding the MSP430X architecture can be found in the MSP430F4xx and MSP430F2xx users guides.

5xx Memory Map

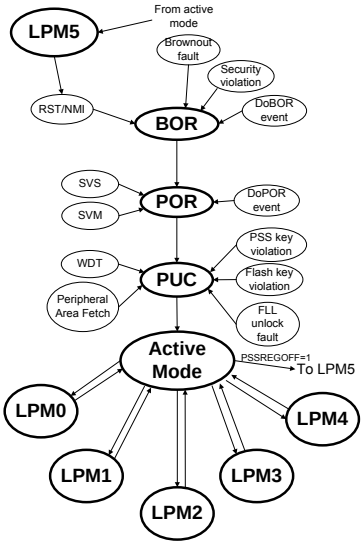
- Page-free 20-bit addressing
- RAM starts at 0x1C00 and is always a contiguous block
- Main flash start moves according to RAM
- Vector table starts at 0xFF80
- User-definable Boot Strap Loader (BSL)

Program	0458FF 010000
Interrupt vectors	00FFFF 00FF80
Program	00FF7F 005C00
RAM 16 KB	005BFF 001C00
Factory data (4 x 128B)	001BFF 001A00
User Info segment A (128 B)	0019FF 001980
User Info segment B (128 B)	00197F 001900
User Info segment C (128 B)	0018FF 001880
User Info segment D (128 B)	00187F 001800
BSL segment 3 (512 B)	0017FF 001600
BSL segment 2 (512 B)	0015FF 001400
BSL segment 1 (512 B)	0013FF 001200
BSL segment 0 (512 B)	0011FF 001000
Peripherals 4 KB	000FFF 000000

This slide shows some of the specifics

The memory map, like the 2xx and 4xx parts with > 64KB Flash, has kept its Interrupt vectors between 0xFF80 and 0xFFFF. The Factory Data was moved out of the Info segment memory to relieve the required management of any stored calibration constants, and we have made the Boot Strap Loader user-definable. Later in the presentation, we will discuss the new boot-strap loader in greater detail.

5xx Operating Modes



- LPM0 to 4 are the same as previous MSP430 generations
- Additional Mode: LPM5
- BOR resets device, executes internal boot code, registers default
- SVS and SVM generate POR in event of low voltage

This is a state diagram of the 5xx operating modes. If you know the previous MSP430 families, you should recognize the POR, PUC, ACTIVE & LOW POWER modes. The two additions are the BOR, LPM5, and some of the reset triggers. The BOR is not new, but rather re-classified as a deeper level of reset. It is always active, monitoring a Vcc voltage drop below 1.8V. LPM5, however, is a completely new concept for MSP430. Having integrated an LDO to separate the core voltage from the peripherals, the MSP430 now has the option to disable those peripherals entirely. This is useful for shelf-life applications when you want the microcontroller to rest in an extremely low-power state until a button is pressed, much like LPM4 is used all other MSP430 families today.

Two new triggers of a POR reset that should be highlighted include the SVS and SVM flags. These stem from the additional voltage monitoring designed into a new Power Management Module (PMM) for the 5xx, that sets a POR signal when a voltage dips below the SVS level and resets the POR signal when it climbs to a slightly higher SVM level, providing hysteresis for the voltage monitor.

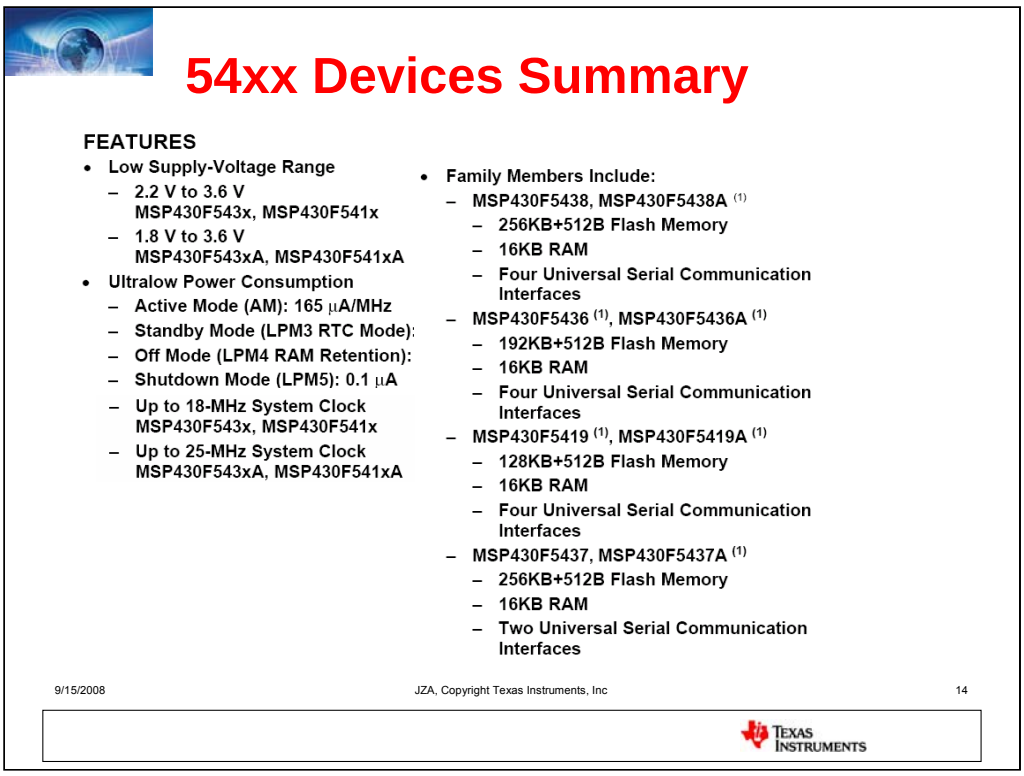
LPM5 Usage

- All I/Os become inputs when regulator shuts down
- RAM is not retained: includes peripheral memory
- On ‘F5438, wakeup only from RST
  - Edges on I/Os have no effect
- All registers – including port registers – get reset when exiting LPM5
- Provided for deep-sleep functionality w/ wake-on-RST
  - Long shelf-life applications

This slide discusses the tradeoffs that should be consider for LPM5. Remember that all voltage to the peripherals is removed. Therefore, the application needs to consider the impact of losing the contents of RAM, which is considered a non-CPU peripheral, such as the stack contents or peripheral register settings. This includes port pins, which reset to an input state. This includes communication peripherals, analog peripherals... All should be accounted for in an explicit initialization routine if one is to enter LPM5 during the application.

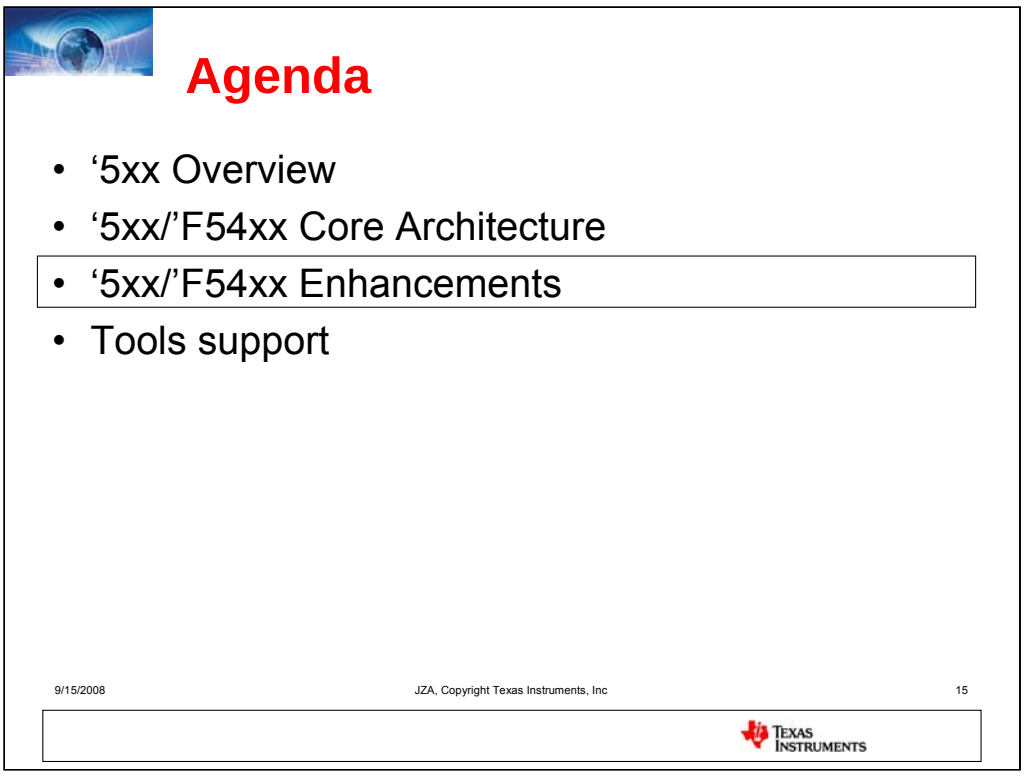
Therefore, we find that LPM5 is best used for shelf-life applications where the user can trigger an edge on the RST pin and wake the part into normal operating functionality.

** NOTE: this should be changed for the released part, due to the fact that peripheral pins will be able to wake the 5xx from LMP5 ***



This is an excerpt from the 54xx datasheet, our first sub-family of 5xx parts. To the right, the slide portrays the differences between different flavors of the 54xx sub-family, including the amount of Flash, number of communications peripherals, and pinout (not shown).

To the left, we show the differences between the F54xx and the F54xxA parts. This is a mainly a distinction of performance where the F5438 delivers up to 18 MHz and an operating range down to 2.2V, and the ‘A’ versions offer the full 25 MHz and operating range down to 1.8 V.



Having discussed, from a high level, the differences in the CPU core, memory map, and operating modes, we can now take a closer look at the peripheral enhancements that have enabled these great leaps in performance and functionality, proving the 5xx to be a truly innovative solution for new applications.

5xx Peripheral Upgrades

- ***New***
  - Power Management Module (PMM)
  - Unified Clock System (UCS)
  - System module (SYS)
  - CRC16 module
- ***Enhanced***
  - DMA
  - ADC12
  - RTC
  - Flash Controller/RAM
  - Hardware Multiplier
  - Watch Dog Timer
  - USCI
  - Ports
  - JTAG and Embedded Emulation

There are four new peripherals to discuss including the Power Management Module (see below), a Unified Clock System, a System Module, and a Checksum CRC16 module.

PMM

Power delivery (including 1.8V LDO for digital core)

Programmable Supply Supervision

Programmable Supply Monitoring

UCS

5xx standard

Orthogonal extension of ‘4xx-based FLL+

SYS

Handles interrupts, arbitrates common resource requests (bus)

Includes BSL, NMIs, etc. (*Now it has a name!*)

Then we have here the list of peripherals that have been enhanced for increased flexibility, robustness, or power consumption. One of the things we are really proud to communicate about the enhancements we have made - in the peripherals, in the new modules, in the power consumption and performance advantage due to these changes, and even in cost - is the achievement of maintaining the look and feel of previous 430 families. There have been no fundamental changes to how someone uses the part, only improved flexibility and performance for the part.

New!

Power Management Module

- V_{CC}: 1.8V to 3.6V
- Integrated LDO: $V_{CC} \rightarrow V_{CORE}$
- Zero-power BOR
- V_{CORE} programmable to four levels
  - 1.35V, 1.55V, 1.75V, 1.85V
- Password protected
  - Lock: PMMCTL_H = 0xA5
  - Unlock: PMMCTL_H = 0x00
- Integrated *Supervision* and *Monitoring*
  - *Monitoring* provides interrupts on event occurrence
  - *Supervision* generates POR if low-voltage event occurs
- Additional accurate voltage supervision for cost of ~100nA

The Power Management module, or PMM, has two main functions:

-To control the programmable LDO separating the peripheral and core voltages, also referred to as V_high and V_low, respectively

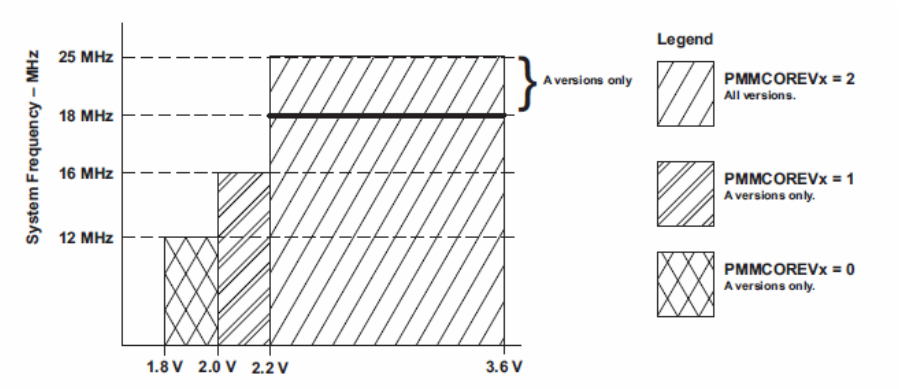
-To monitor those voltages using the always-on BOR, and the optional Supply Voltage Supervisor (SVS) and Supply Voltage Monitor (SVM)

All PMM registers are password protected to make each application more robust – meaning core voltage and voltage supervisor levels cannot be accidentally edited during operation. The PMM registers can only be written when the PMM is unlocked. The LDO provides three programmable levels for Vcore, allowing the user to match power consumption vs. required processing performance.

Each one of these Vcore levels have a respective SVS and SVM setting to monitor that the supplied voltage matches the expected setting for the application. This does not mean, however, that Vcc is no longer able to be monitored, as is possible in previous families. In fact, the SVS and SVM are programmable to monitor a high-side setting (for Vcc and peripheral operation), as well as the low side (for the CPU).

New!

Power Management Module



Most applications can operate at lowest setting, with no need to alter default PMM configurations

This shows the relationship between the core voltage settings and the resulting performance. At the lowest Vcore setting, and across the entire operating range of the device, the MSP4305xx family can provide a full 12 MHz of CPU performance! Each step in the Vcore then delivers increasing speed, but this is a ground-breaking gain in performance over our previous families, that do not integrate an LDO and are, therefore, subject to the curve of frequency vs voltage.

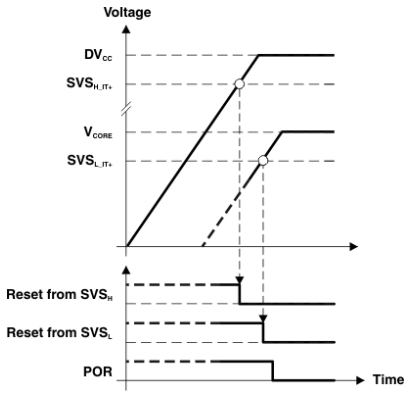
One important note here is the mention of ‘A’ versions only for PMM settings one and two. The operating range for the non-A version of the F54xx sub-family is specified down to only 2.2V because flash access is not reliable over the entire operating range for Vcore settings less than two, which would be required at Vcc < 2.2V.

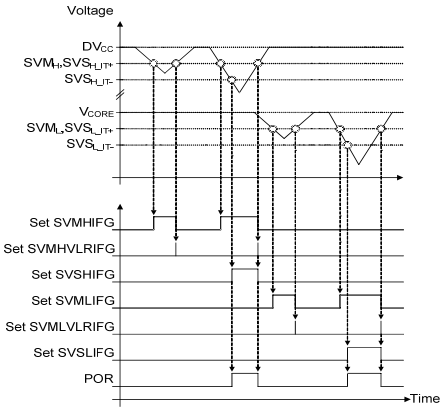
This is important because the default setting for the PMM is zero. Therefore, any application using the F54xx, non-A version, needs to increase the core voltage level to level 2 before executing any application code. To do so, TI provides a PMM software library with API’s to increase and decrease the voltage levels accordingly.

New!

Supervision / Monitoring

- Flags automatically set/cleared according to rail state
- SVM, SVS, BOR are working hand in hand
- POR event generated as well



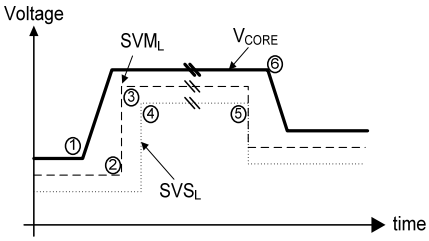


The SVS and SVM capabilities of the PMM allow us As Vcore changes and we want to make sure that the voltage does not go below what we require for correct operation, or when we want to monitor Vcc for a certain voltage level, say, because you want to know if AVcc dips below the 2.5V to supply the voltage reference of your ADC12, the new SVS and SVM monitors can deliver added robustness for just 100 nA of added current consumption.

New!

5xx PMM Software: Changing V_{CORE}

- Set and check the required V_{CORE} voltage before increasing the CPU frequency
- Increase/decrease V_{CORE} only step by step
- See example below:

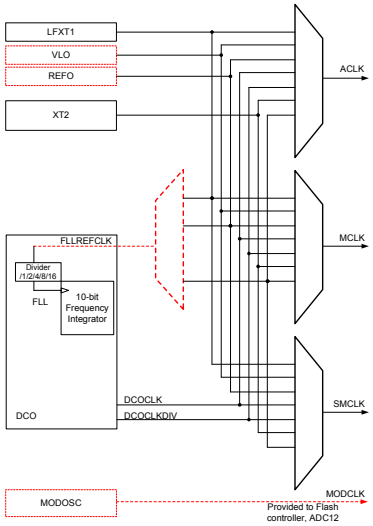



```
PMMCTL0_H = 0xA5;                       // Open PMM module
PMMCTL0 = 0xA500 + level;               // Set VCore
SVSMLCTL = SVMLE + (level * SVSMLRRL0);// Set SVM new Level
while ((PMMIFG & SVSMLDLYIFG) == 0);    // Wait till SVM is settled (Delay)
PMMIFG &= ~(SVMLVLRIFG + SVMLIFG);      // Clear already set flags
if ((PMMIFG & SVMLIFG))
  while ((PMMIFG & SVMLVLRIFG) == 0);   // Wait till level is reached
PMMCTL0_H = 0x00;                       // Lock PMM module registers
// Change DCO speed here
```

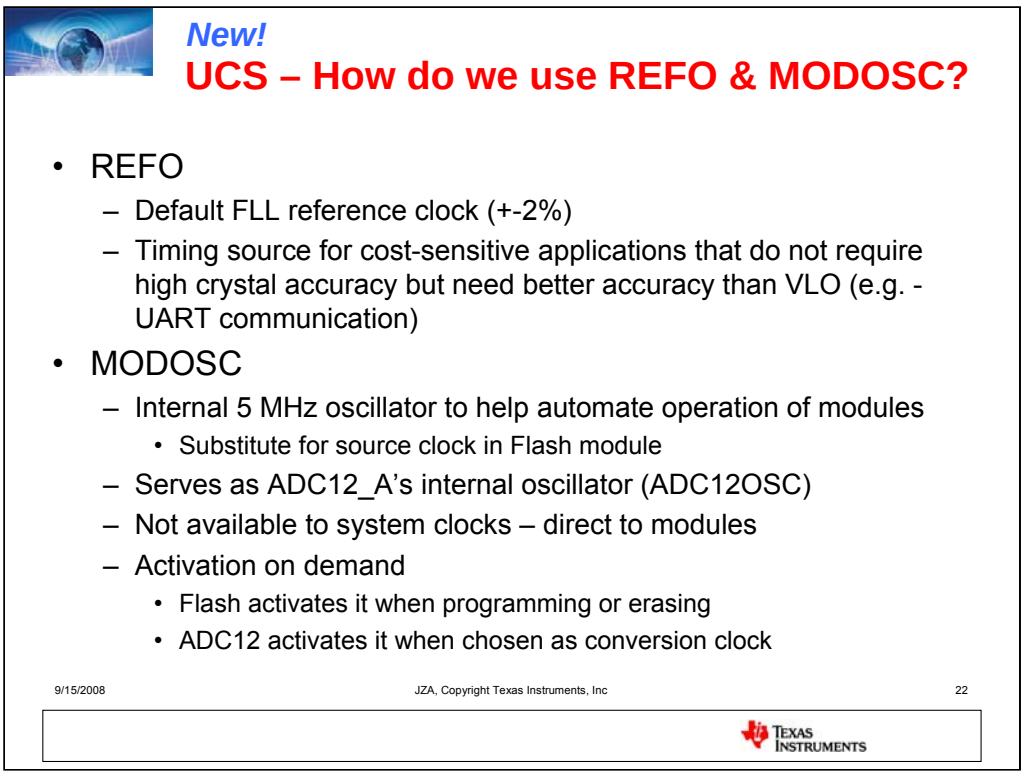
New!

F5xx Unified Clock System (UCS)

- 6 independent clock sources
  - Low Freq
    - LFXT1, VLO, REFO
  - High Freq
    - XT2
    - DCO – optional FLL
    - MODOSC
- FLL reference selectable from three, divisible low-freq sources
    - LFXT1
    - VL0
    - REFO
- MODOSC provided to modules
  - Flash controller & ADC12
- ACLK/SMCLK/MCLK can be driven from any source
- Clocks on demand



ACLK/SMCLK/MCLK can all be driven from any source



REFO

Can you do RTC with REFO? Not really → +/-2% error means +/- 1/2 hour error every day

NOTE:

Power draw is higher than crystal or VLO

Is the default FLL reference clock

MODOSC

No configuration of f_{FTG} required because of new Flash module

Great for applications in which drift isn't critical

New!

Oscillator Fault / Fail-Safe Modes

- Fault detection (XT1, DCO, XT2)
  - Flag set if oscillator enabled but not operating properly
  - Crystal oscillator clocks will switch to safe backup clock
    - LFXT1 reverts to REFO
    - HFXT1/XT2 reverts to DCO
    - WDT reverts to VLO
  - Improvement from 2xx/4xx Families
    - LFXT1 would revert to DCO → freq difference is significant
- During an oscillator fault, DCOCLK active even at lowest DCO tap, to provide clock for the CPU

-Extended the fault detection capabilities to include XT2 and to automatically change to safe backup clock.

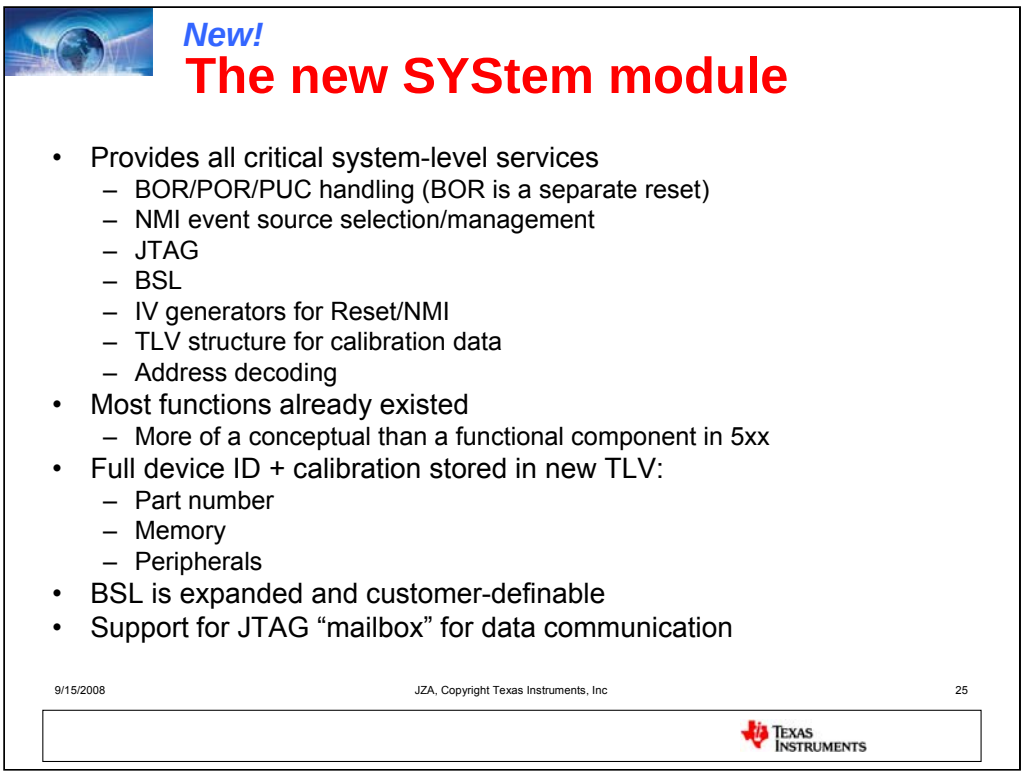
- Fail-safe modes ensure minimal operation if primary clock source fails

New!

Review of Available Clocks

Clock	Frequency (nominal)	Precision	Current Draw	Crystal Required
High-Frequency				
DCO	**100kHz – 32MHz**	**Low**	**60uA**	
HFXT1/2	**4 - 32MHz**	**High**	**60uA @ 12MHz**	**X**
MODOSC	**5MHz**	**n/a**	**n/a**	
Low-Frequency				
LFXT1	**32kHz**	**High**	**300nA**	**X**
VLO	**12kHz**	**Low**	**0nA***	
REFO	**32kHz**	**Medium/High**	**3uA**	

* Included in $I_{LPM3, VLO}$ spec (~1.2uA)



TLV structure is contained in a dedicated memory region, apart from INFO mem

Described through Tag-Length Value (TLV) structure

Describes device’s capabilities

- Exact device derivative
- Memory size
- Peripheral availability

Contains factory-provided calibration data, e.g.:

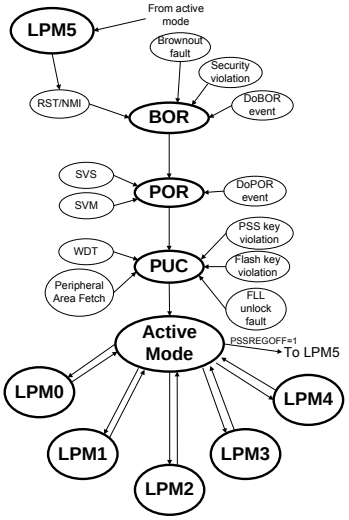
- ADC offset voltage
- ADC temperature sensor calibration data

Same app build can run on different devices by detecting capabilities and adjusting functionality

New!

BOR / POR / PUC Sources

- BOR Sources:
  - Power on / Brownout
  - RST/NMI
  - Security violation (protected Memory)
  - Software (Bit in PMM)
  - LPM5 wake up
- POR Sources:
  - SVS low/high
  - Software (Bit in PMM)
- PUC Sources:
  - WDT
  - Key Violation (WDT, Flash, PMM, …)
  - Fetch out of Peripheral Area
  - Software (Bit in PMM)



New!

System Reset Interrupt Vector Generator

- New interrupt vector generator register SYSRSTIV simplifies handling
- SYSRSTIV contains the cause of last reset
- 17 possible reset causes recorded
- Writing to SYSRSTIV automatically clears all flags
- Brownout Reset (BOR) now treated as a reset state
  - Deeper than PUC reset

Brownout (BOR) (highest priority)
RST/NMI (POR)
DoBOR (BOR)
Port_wakeup (BOR)
Port_wakeup (BOR)
Security violation (BOR)
SVSH (POR)
SVML_OVP (POR)
SVMH_OVP (POR)
DoPOR (POR)
WDT time out (PUC)
WDT key violation (PUC)
KEYV flash key violation (PUC)
PLL unlock (PUC)
PERF peripheral/config area fetch (PUC)
PSS key violation (PUC)

Texas Instruments

Interrupt Vector Generator - many interrupt flags available in single register

Simplifies code for execution & efficiency

5xx makes extensive use of Interrupt Vector Generator Registers, not just for the SYS module.

Timer_A/B, ADC12, RTC, NMIs, Resets, Ports, DMA, USCI

New!

NMIs: Non-Maskable Interrupts

- Now divided into two types: SYSTEM & USER
- System: Highest priority
  - SYSSNIV IV register for handling
  - PMM high-side or low-side supervisor low-voltage fault
  - PMM timeout
  - Access to vacant memory
  - JTAG mailbox event
- User: Next priority
  - SYSUNIV IV register for handling
  - Edge on RST/NMI pin
  - Oscillator fault
  - Flash access violation

New!

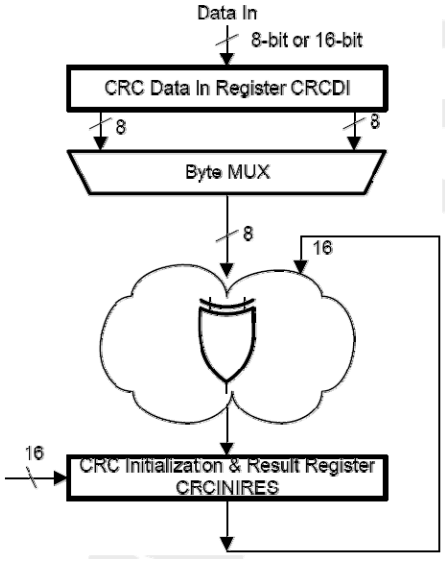
Device Protection / Robustness

- Consecutive system NMIs (storms) allow one cycle of main( ) execution in between handling
- System Module prevents access of protected memory area (including JTAG or DMA)
  - Illegal memory access causes NMI
- Password protection of all critical control registers (Power Management Module, RAMCTL, Flash Controller, Watchdog, etc.)

New!

CRC16 Module

- Single-cycle execution
- Based on CRC-CCITT standard
- Easy to use:
  Write value to register → read output in next cycle
- Use with DMA to generate Flash checksums with minimum CPU overhead



USCI Enhanced Features

- Interrupts re-designed
  - Separate vectors for USCI_A & USCI_B – no more sharing or bit-testing
  - Interrupt vector generator register
  - Simplifies USCI interrupt operations
  - Reduces code size

UCBxIV, USCI_Bx Interrupt Vector Register

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
0	0	0	0	UCIVx			0
r0	r0	r0	r0	r-0	r-0	r-0	r0

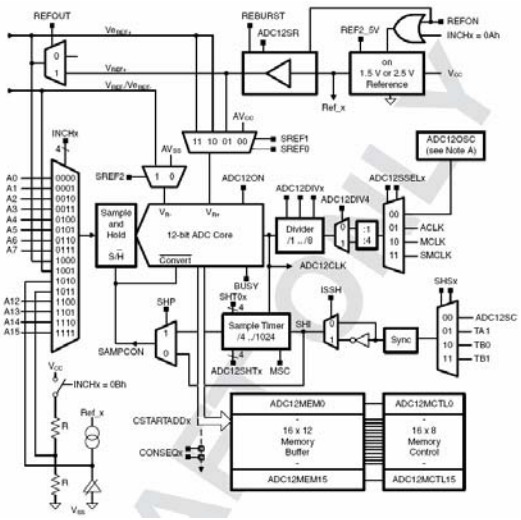
UCIVx Bits 15-0 USCI interrupt vector value

UCBxIV Contents	Interrupt Source	Interrupt Flag	Interrupt Priority
000h	No interrupt pending	–	
002h	Arbitration lost	UCALIFG	Highest
004h	Not acknowledgement	UCNACKIFG	
006h	Start condition received	UCSTTIFG	
008h	Stop condition received	UCSTPIFG	
00Ah	Data received	UCRXIFG	
00Ch	Transmit buffer empty	UCTXIFG	Lowest

Improved!

ADC12_A Enhanced Features

- VREF settles in 50us instead of 17ms
- Tighter temp coefficient on internal reference (±100 vs. ±50ppm)
- Lower power modes
  - Selectable speed vs power mode
  - References automatically shut down to conserve power
- Higher clock dividers for faster system clocks
- ~6x lower current! (vs ADC12)
  - ***220uA for ADC active***
  - ***100uA for 2.5V VREF active***



New pre-divider available

Not an issue unless you use the faster clock speeds

Tighter temp coefficient on internal reference (±100 vs. ±50ppm)

Consider new power-saving features in ADC12CTL2 register

VREF settles in 50us instead of 17ms

Improved!

5xx Generation Embedded Emulation

- Up to 8 hardware breakpoints with complex trigger capability
- 40-bit wide CPU cycle counters in hardware
- Mailbox system provides direct interface to the CPU during…
  - Debugging (Run-time data exchange – RTDX)
  - Programming / Test
- State Storage: non-intrusive trace buffer for data and address bus (e.g., instruction fetch etc.)

Agenda

- ‘5xx Overview
- ‘5xx/’F54xx Core Architecture
- ‘5xx/’F54xx Enhancements
- Tools support

Improved!

5xx Generation JTAG

- Primary interface for ISP and emulation
- JTAG access can be “locked” in user SW
- JTAG pins can be used as I/Os
- 5xx devices support both 4-wire and 2-wire (“Spy-Bi-Wire”) JTAG protocols
- Compatible with existing MSP430 tools, e.g. USBFET:

JTAG can be “locked” in software – making only public JTAG instructions available (device ID, mailbox, etc.)

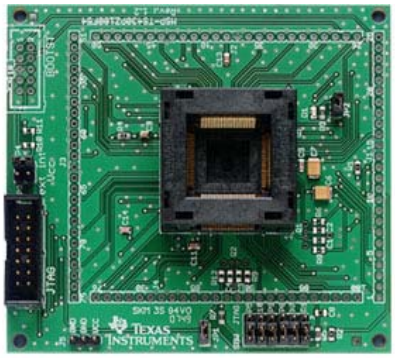
Lock is initiated from user code through the API of the integrated TI-provided boot strap loader

Lock is irreversible

No physical JTAG fuse to burn

5xx Flash Emulation Tool (FET) Board

- 100-pin target board exclusive to the 5xx devices
- Development board with 100-pin TSSOP (PW) ZIF socket (MSP-TS430PZ5x100)
- All pins brought out to pin headers for easy access
- Programming via JTAG, Spy-bi-wire or BSL
- *$49 only*

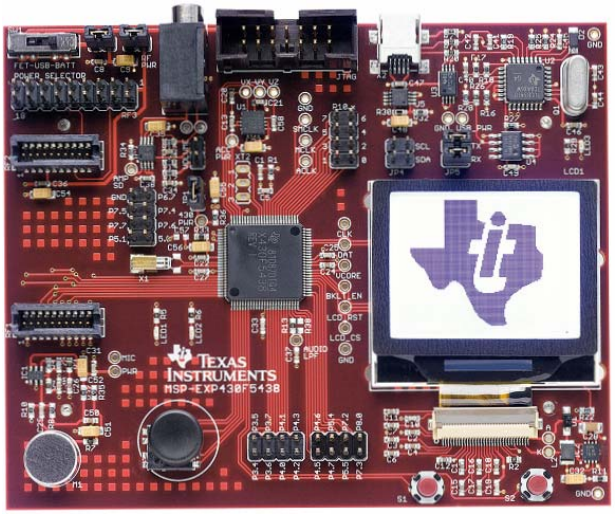


MSP430F5xx 100-pin Target Board
MSP-TS430PZ5x100

The Hardware: MSP-EXP430F5438

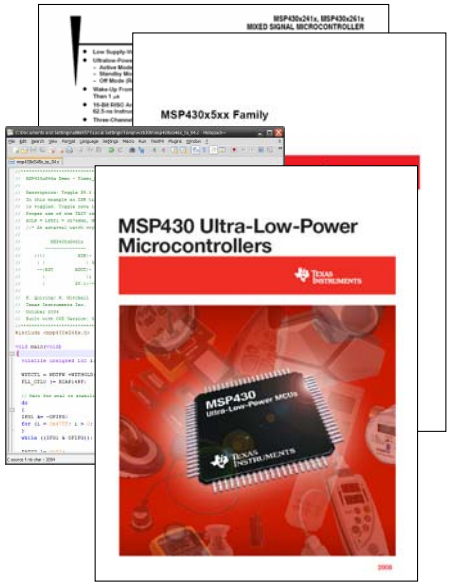
- MSP430F5438 platform
- Easy power select
  - USB, JTAG, Battery
- USB comm. & power
- Microphone
- Filtered PWM audio output
  - Active, selectable gain
  - Headphone compatibility
- X / Y / (Z) accelerometer
- Dot Matrix LCD (138x110)
  - Integrated backlight
- 1 x 5-way switch
  - (L, R, U, D, C)
- 2 x push-button switches
- RF Interface
  - CC EMK I/F
  - EZRF I/F (18- pin)
- 2 x AA batteries

AVAILABLE 4Q '08



www.ti.com/msp430

- User's Guides
- Datasheets
- Code Libraries
- 100+ Application Reports
- 1000+ Code Examples
- Product Brochure
- Latest Tool Software
- 3rd Party Listing
- Silicon Errata



TEXAS INSTRUMENTS

The 430 is very well supported including a dedicated TI website www.ti.com/msp430.

For detailed technical information on device peripherals, TI has up-to-date MSP430 Family User's Guides available.

Chip specific electrical and pin information is available in device-specific datasheets.

Over 100+ application reports and 500+ downloadable code examples are available from the MSP430 website.

The product brochure provides a description and an overview of all available MSP430 devices.

A listing of 3rd parties is provided.

Any known silicon errata is available.

A FAQ system (Knowledge Base) and regional technical support phone lines also are available.

The most current MSP430 documentation is always available on the MSP430 website.

Thank you!