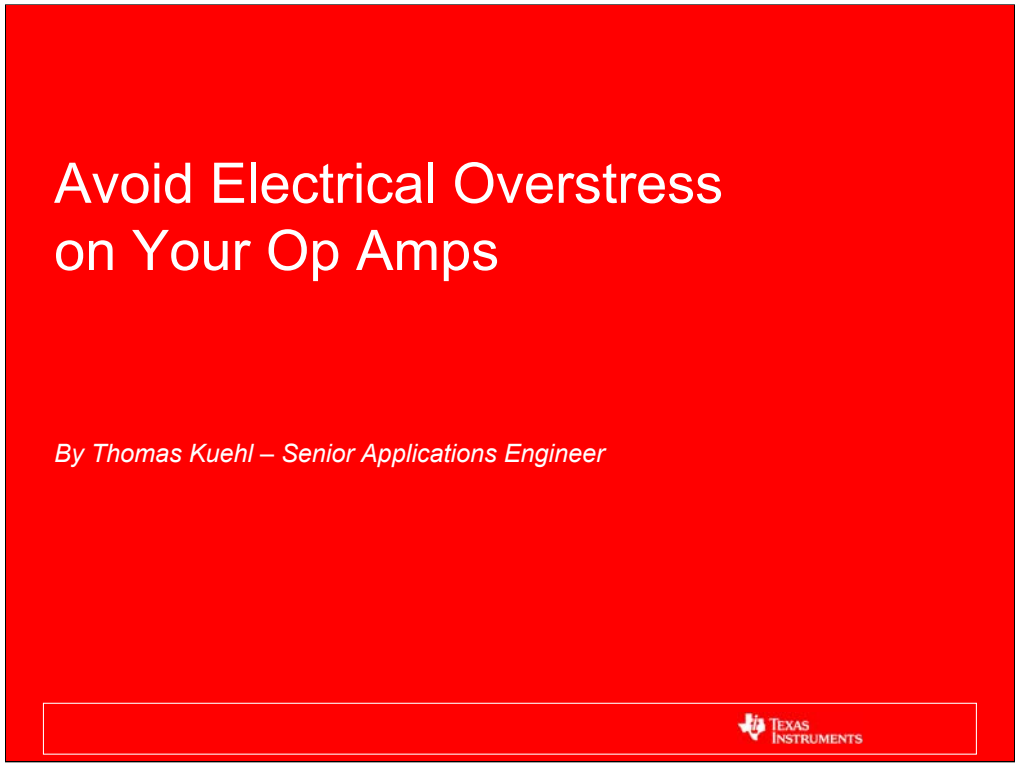
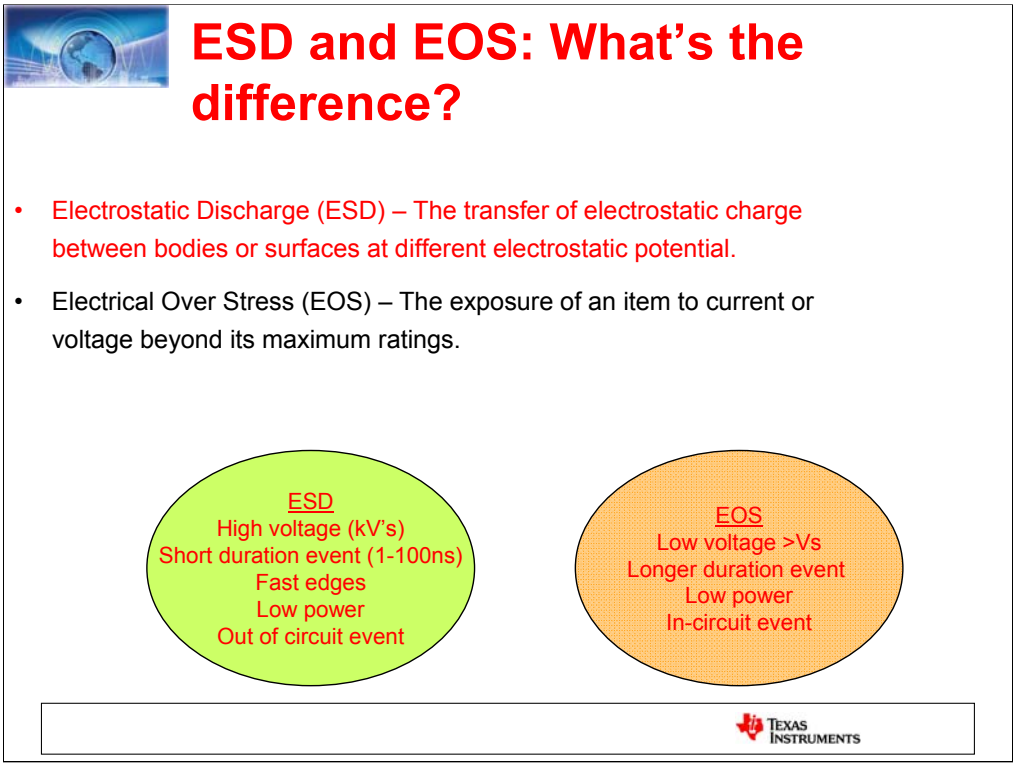


The presentation today will examine the issue of input electrical overstress. Simply, this implies a condition where potentials applied to the amplifier exceeds those of the normal specified operating range. Most circuit applications will never experience an input or supply overstress, but in those few cases where there is the potential for an overstress condition it is important to understand the performance or reliability implications.

Presentation Subjects

- ESD and EOS definitions
- Amplifier input range
- ESD models
- Internal ESD and consequently EOS protection circuits
- Amplifier EOS operating situations
- External EOS protection



One of the most intuitively evident sources of electrical overstress is Electrostatic Discharge, ESD. An ESD event can take place when two bodies are at 2 different electrostatic potentials; often thousands of volts apart. If a conductive path is provided between the two bodies, a transfer of electrostatic charge can take place until charge neutrality is achieved.

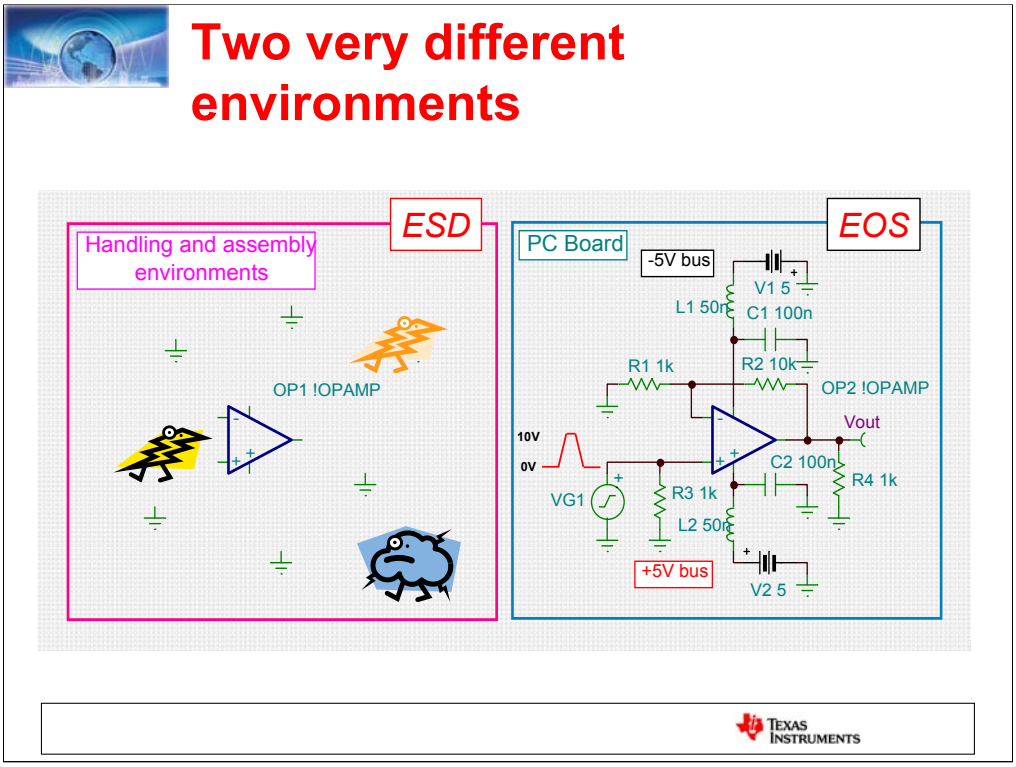
The event usually takes place in a fraction of second; less than 100ns. An electrostatic EMF on the order of kilovolts can be reduced to zero during the brief charge transfer period. Current on the order of amperes may flow through the path if there is little opposition to current low. Remember:

$$i(t) = C \cdot dV / dt$$

Decades ago semiconductor circuits fell victim to ESD events resulting in complete circuit failure, or even more hideous parametric degradation. However, since that time ESD has been well characterized, better understood and protection solutions implemented.

Input Electrical Overstress, EOS, is likely an unintentional application of an over-voltage typically outside the normal operating range and much longer in duration than an ESD event. An important point to keep in mind is that this is an in-circuit event, while ESD is usually an out-of-circuit event.

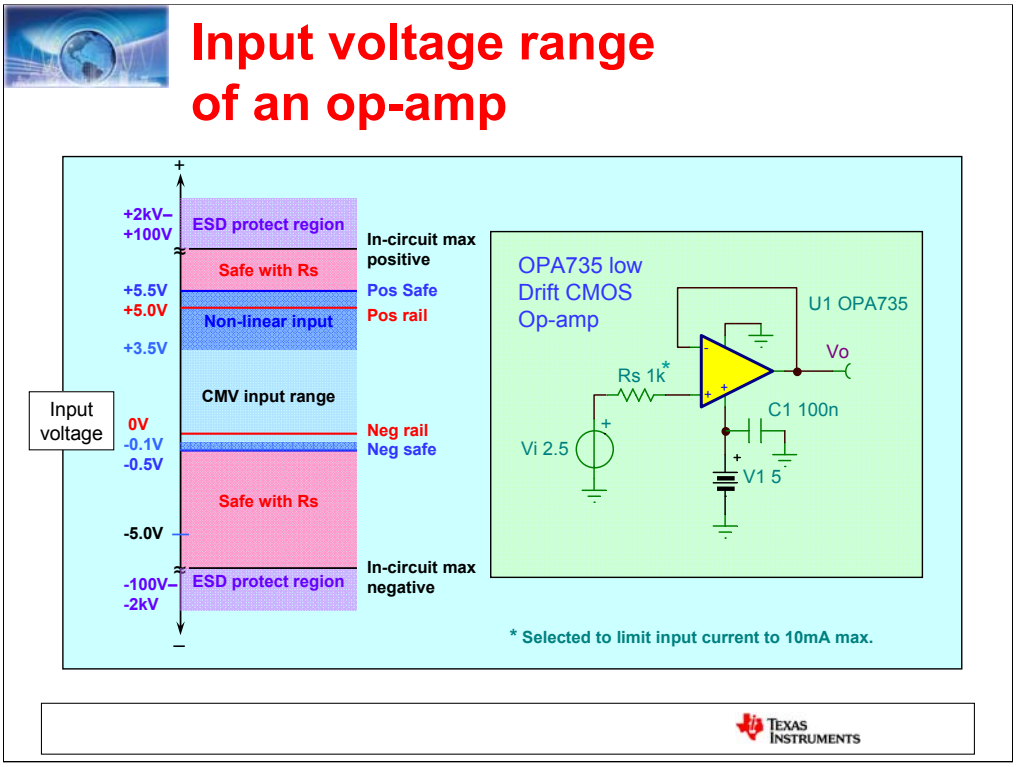
Unknowingly we may be relying on a device's internal ESD circuits to provide protection during an EOS event as well.



Internal ESD protection circuits are primarily intended for pre-assembly handling and assembly operations. Low impedance ground paths abound which can serve as discharge paths. But once the IC is installed in the PC board and interconnected to other components the likelihood that an ESD path exists is greatly diminished. There is every possibility that with proper ESD control and prevention that the internal ESD circuitry will never be exercised. That is a good thing!

However, there is the other possibility that a device input may be subjected to an EOS event while installed in the operating environment. And although the ESD circuitry may not be specifically designed for a particular EOS condition, there is a probability that it will come into play during the event.

This circuitry could provide a protective path for the input devices where no damage to the circuit ever occurs. Or, at the other extreme, it could be damaged and become a liability to the otherwise normally operating circuit.



The scale on the left side of the slide depicts the input range for the OPA735 CMOS op-amp. The linear response CMV region is stated as -0.1V to +3.5V. Exceeding these values by any appreciable amount will result in signal distortion.

Moving in the positive direction, from +3.5V to +5.5V, the input is still within a safe region, but signal linearity will suffer becoming increasingly worse. Note that the positive supply rail is +5.0V, so an input signal more than about 0.5V beyond this results in the positive ESD diode turning on. A hard turn on begins around +5.5V and a series input resistor must be added to limit the current. The input current is usually restricted to a value of 5 or 10mA. Failure to include the resistor will almost assuredly result in damage to the internal ESD diode if the current becomes too high.

The series resistor can be used to protect the input up to reasonable limits, tens of volts. But be aware the resistor will add noise to the overall circuit performance which may be objectionable from a performance stand point. Note in many applications this resistor is not included.

The series resistor is determined from the maximum applied input voltage, maximum input voltage rating and maximum current:

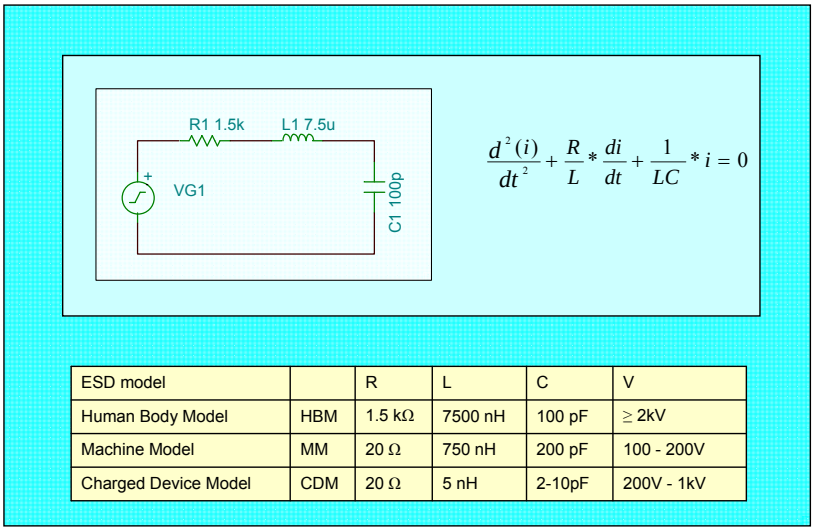
$$R_{SERIES} = (V_{APPLIED\ (MAX)} - V_{INPUT\ (MAX)}) / I_{INPUT\ (MAX)}$$

Be sure to check both the positive and negative input regions. For the above circuit the negative input region will result in a larger value resistor.

In the realm of 100V or more the ESD circuitry is really in place to protect the device during an ESD event. It is not realistic to expect EOS protection at such high voltage levels.

Moving the input about 0.5V beyond the negative rail results in the negative ESD diode turning on. The same precautions as the positive case must then be observed. The remaining negative input conditions mirror those of the positive conditions.

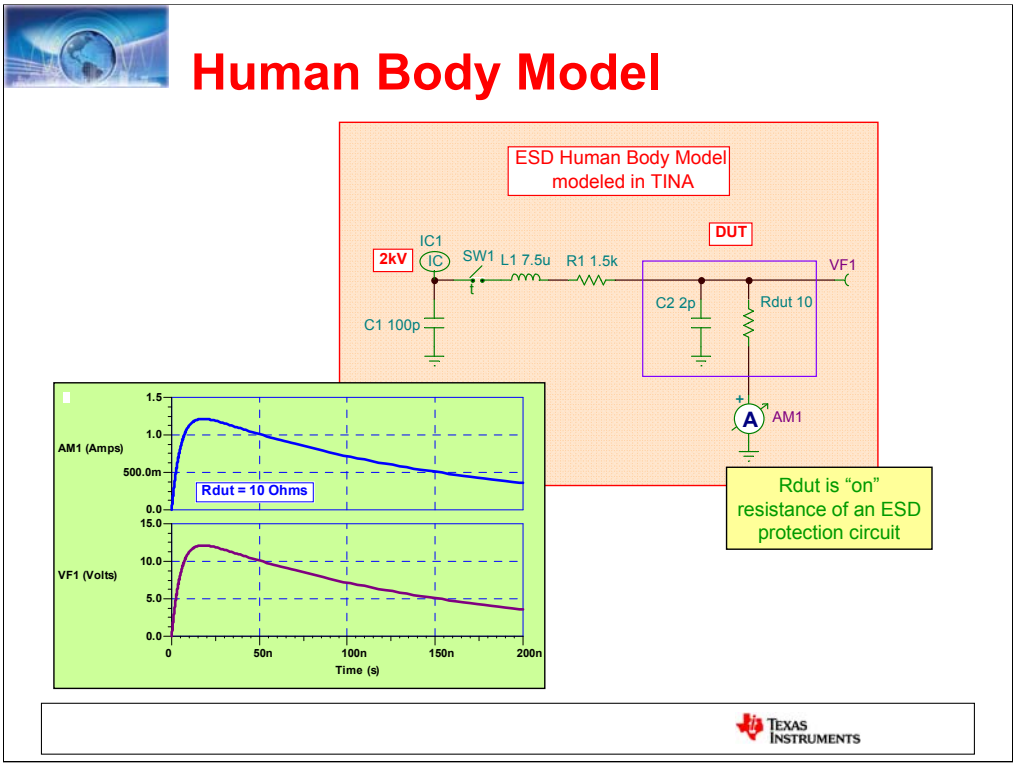
ESD Stress Models



ESD model		R	L	C	V
Human Body Model	HBM	1.5 kΩ	7500 nH	100 pF	≥ 2kV
Machine Model	MM	20 Ω	750 nH	200 pF	100 - 200V
Charged Device Model	CDM	20 Ω	5 nH	2-10pF	200V - 1kV

Texas Instruments

There are 3 different ESD generator models commonly applied when testing semiconductor ESD protection circuitry. They are the Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM). All 3 boil down to a series RLC circuit, but the circuit values and pulse generator characteristics are much different for the 3 models. All 3 produce a short, but well defined ESD pulse that results in current levels comparable to those experienced during an actual ESD event.



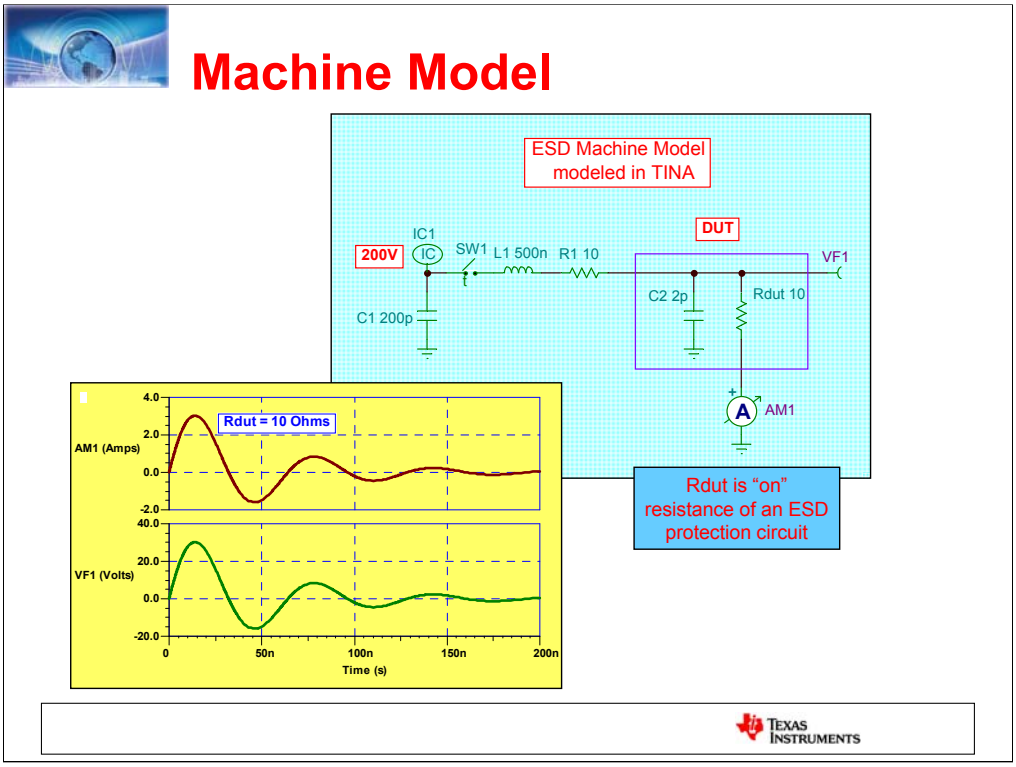
The first model, the Human Body Model (HBM) is intended to simulate an statically charged human touching an IC pin that has a current path to ground.

C1, L1 and R1 represent the charged human electrical properties. C1 holds the high voltage charge which in this case is established at 2kV. When contact is made, the equivalent of SW1 being closed, C1 discharges through L1, R1 and parallel combination of C2 and Rdut – of which the latter 2 components represent the path internal to the IC. The current is defined by the 2nd order differential equation for this circuit. Note that the current peak - Ipk, occurs quickly; under 25ns with a maximum value of 1.2 to 1.3 amperes. However, significant current continues to flow for hundreds of nanoseconds. The integrated power can be surprisingly high during this period and the protection circuitry must be capable of not only withstanding the high voltage associated with the ESD pulse, but also dissipating the power.

Although Rdut is represented by a 10Ω resistor, it is sometimes replaced with a 10V zener diode which exhibits a hard "turn on" characteristic at 10V. The dynamic resistance may be much less 10Ω's.

When a device is characterized using the HBM ESD environment the test is conducted using multiple, increasingly large charge voltage levels. Usually the lowest test level used is 500V, which is then increased 500V until 2kV is reached. Testing may continue to the 3 or 4kV input level.

There are times when the semiconductor process may dictate that a lower starting voltage level be used, in which case it may be as low as 100V. On the other end, semiconductors that have I/O pins routinely exposed to manual, make and break connections may be tested with charge voltages as high as 15kV. HPA products are designed to withstand an HBM ESD voltage of 2kV.

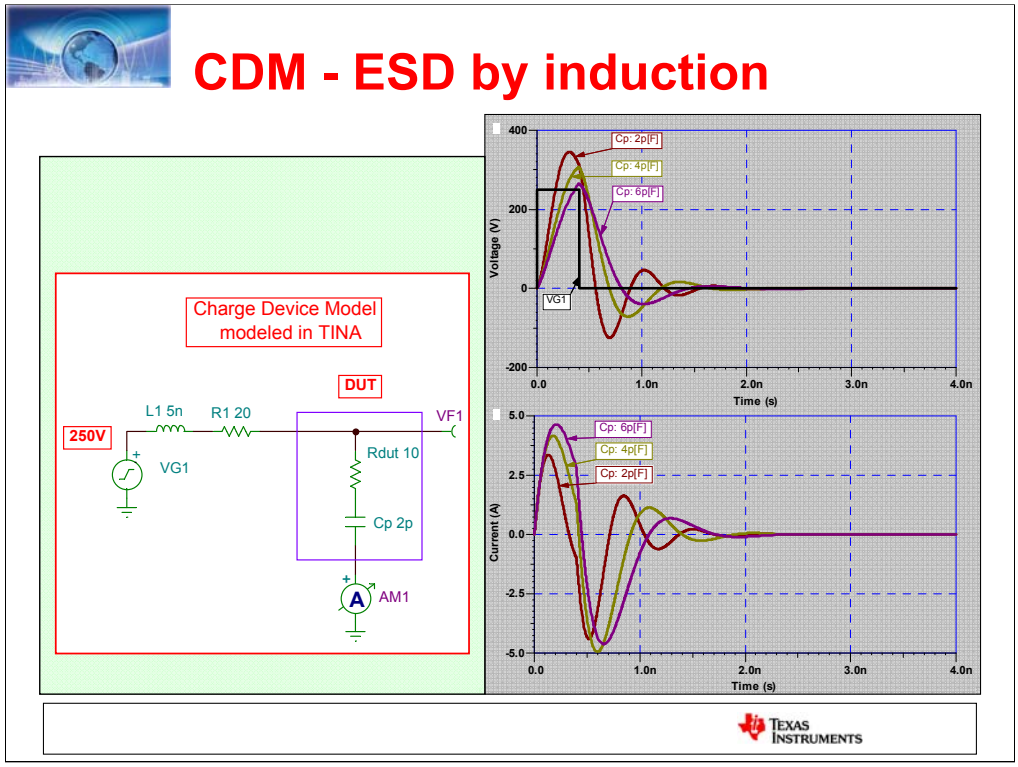


The second model, the Machine Model (MM), was introduced by the Japanese semiconductor industry and was intended to be a more severe test than the HBM. The charge capacitor was made intentionally larger – 200pF, and the charge source resistance reduced to a very low value, 0 to 10Ω. This allows the ESD source to supply even greater currents than the HBM model.

Although this model was intended to represent machines associated with the end user electronic assembly, it is not intended to represent the handlers used in semiconductor final testing and handling. It may simulate the electrical stress from low impedance sources that are not necessarily ESD.

Notice that the charge voltage is 200V, instead of 2kV as with the HBM model. This is dictated by the fact that the current is only limited by the finite source resistance and the "on" resistance of the ESD protection circuit path. Higher voltage would result in dangerously high currents that would almost certainly damage even the most robust ESD circuits. For the example shown the peak current exceeds 2 amperes on the positive peak and then follows a damped pulse response from there. The entire event concludes in about 200ns, which is substantially less than the HBM event's duration. That noted, it is important to recognize that the integrated power dissipation is higher and occurs in a shorter time period. Passing the MM test is usually a more difficult feat than than passing the HBM test. The MM test is conducted with a starting voltage of 100V, which is advanced 50V at time to 200V.

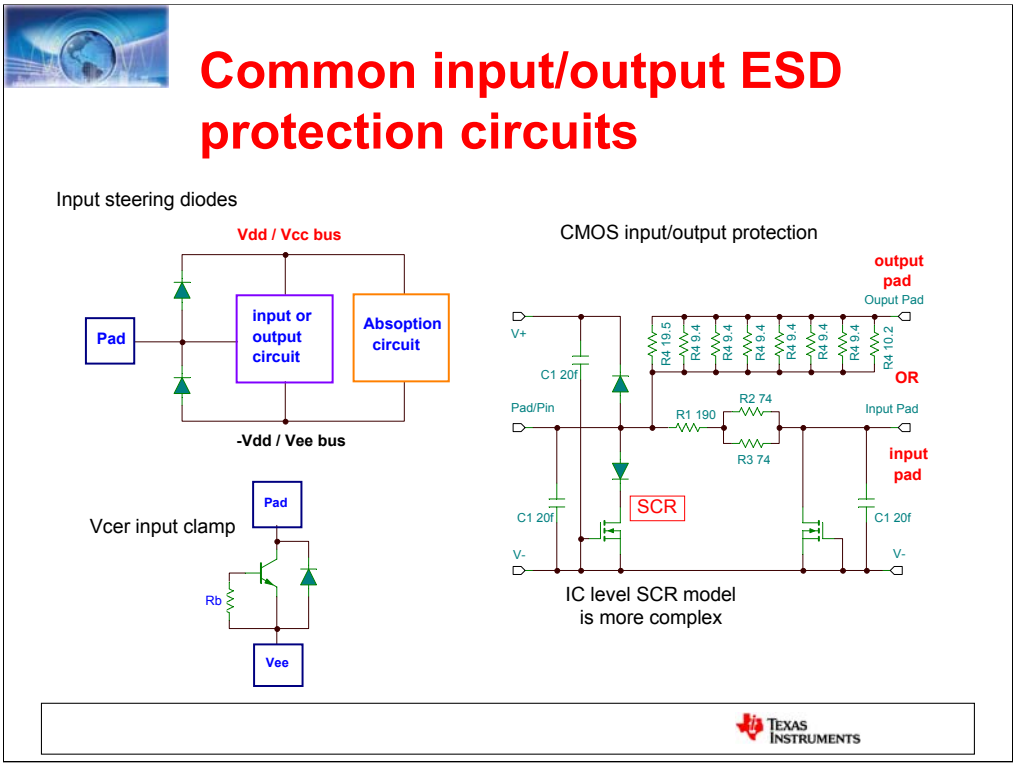
As was mentioned, the MM may actually better model a low impedance, HV source, than an actual ESD source. Therefore, the MM qualification has been dropped by the US and Europe as a requirement. Only Japan continues to require MM qualification of products.



The third commonly employed ESD model is the Charge Device Model (CDM). It has come to replace the one time popularly applied MM. This model is specifically slated to simulate the charge accumulated by an IC package, or piece of manufacturing equipment, as a device is processed through the final production operations.

The CDM charge voltage is set to 250V. The pulse width is very short; less than 400ps with extremely fast edges. Like the MM the series resistance is low. The device under test (DUT) model consists of the ESD protection “on resistance” and a small value series capacitor. The CDM model is a charged package model where the small capacitor is the die/package to the surrounding manufacturing environment capacitance. Therefore, the capacitance value depends on factors such as the die size, package size, dielectric characteristics and surrounding environment characteristics.

Once the ESD pulse is initiated the current rapidly rises to a value dependent on the said characteristics. The plot shows the resulting current waveform for different package capacitances; 2, 4 and 6pF. The capacitance value somewhat alters the peak current and settling time. For the example shown the peak current approaches 5 amperes, but note that the entire event is over very quickly - in less than 2ns.

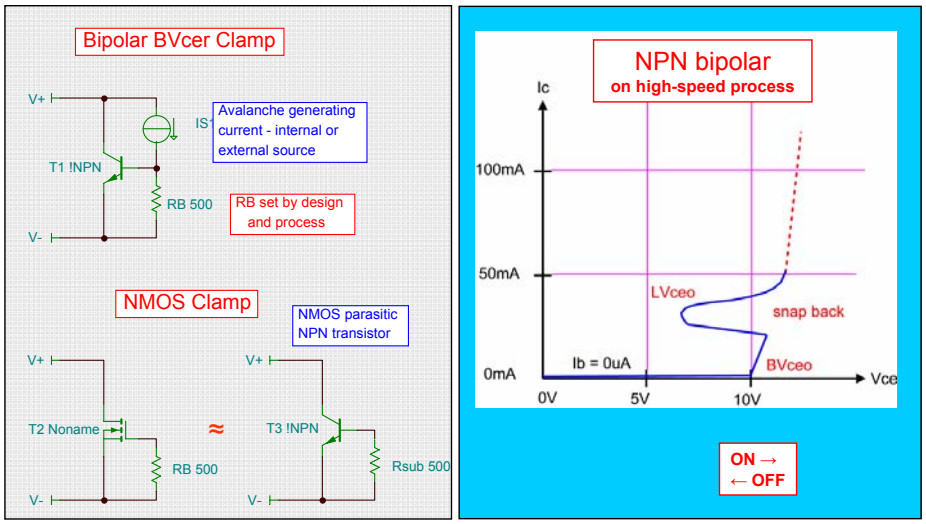


A commonly applied practice for protecting both bipolar and CMOS input and output pads involves steering diodes and an absorption circuit. Depending on the ESD pulse polarity one or the other diode will turn on and the current will be directed through the absorption circuit. This circuit is “off” when the IC is in operation, but momentarily turns “on” during an ESD event. It is intended to absorb the ESD event energy and then dissipate it as heat.

The Vcer clamp circuit relies on the breakdown of the NPN transistor for a positive going ESD pulse and diode conduction for a negative going pulse.

The third circuit is typical of one used to protect CMOS IC inputs and outputs. Although the schematic shows a simple series connected MOSFET-diode clamp at across the input to the ground bus, the physical layout of the IC has parasitic structures that form a true 4-layer, SCR device. SCRs have faster turn-on times than the simple breakdown connected MOSFET. The circuit has a secondary protection path consisting of some series absorption resistors and a clamp MOSFET for the input circuit.

Supply clamp circuits

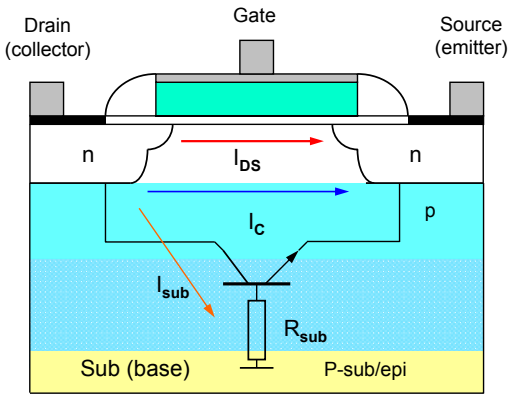


The power supply clamp circuit is satisfied using a bipolar transistor or by a parasitic bipolar transistor inherent to an MOS device. The clamp transistor's base-emitter junction is not forward biased (IB =0uA) rendering the device in a normally "OFF" state.

As the collector-emitter voltage is increased, the breakdown voltage (BVcer) is approached. The internal electric field intensities increasing to a level where electron-hole pairs are generated and current begins to flow between the collector and emitter. If the collector-emitter voltage is further increased the collector current rapidly increases until the point is reached where a "snap back" takes place. This is due to impact ionization and the resulting regenerative feedback. Beyond the snap region current again begins to rapidly increase.

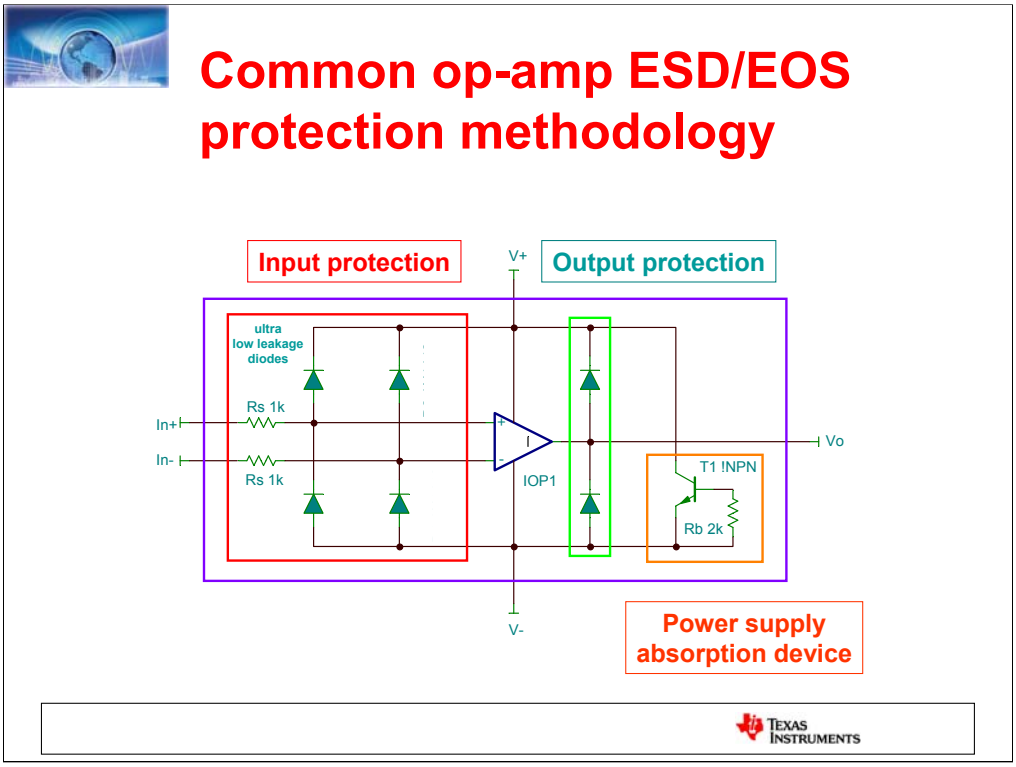
If there isn't another source of resistance in the transistor's path to limit the current, it can increase to the point where the thermal regeneration results in excessively high temperatures and transistor melt down. Usually the emitter ends up spiking through the base and shorting to the collector forming a permanent short circuit.

NMOS parasitic bipolar transistor



Texas Instruments

This is a cut away, side view of an NMOS clamp structure. The parasitic NPN transistor is revealed within the NMOS structure. In normal operation the parasitic bipolar does not function. However, under the previously described conditions, the device will latch in the on state.

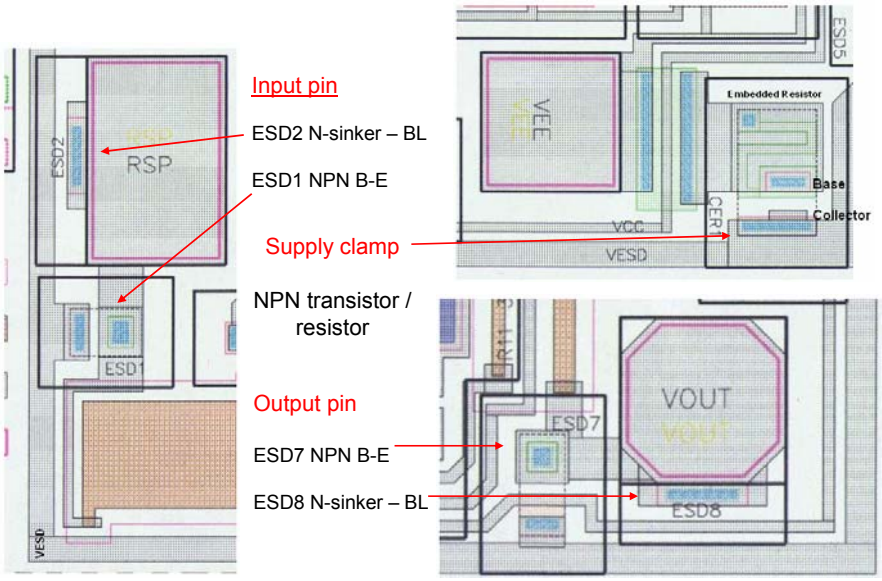


This is a typical ESD protection scheme for an analog circuit. Integrated diodes are connected from each input and the output pins back to each supply rail, V+ and V-. An internal series resistance may be placed in each input path to limit the current during an ESD event. This resistance may be a diffused element or simply the resistance of metal or poly interconnections.

The output protection devices may be larger area devices compared to an input protection device. Most op-amps have minimal resistance between the output devices and the output pin. Resistance in this path will limit output current and output voltage swing during heavier output current conditions.

The other protection element is an absorption device connect between the positive and negative supply pins. It is a large area transistor and if triggered on, it can handle the current directed to it by the input/output steering diodes and then dissipate the momentary energy release without damage. This transistor's collector-emitter breakdown exceeds the maximum rated supply voltage for the device and should only turn "on" during an ESD event.

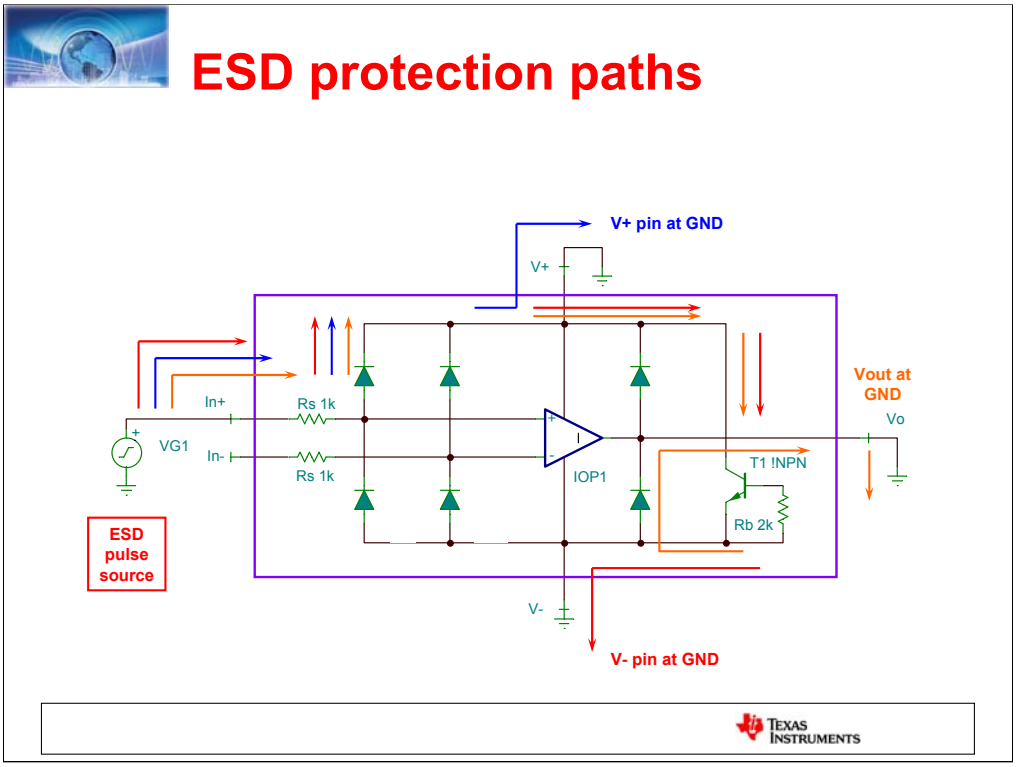
INA168 ESD cell layouts



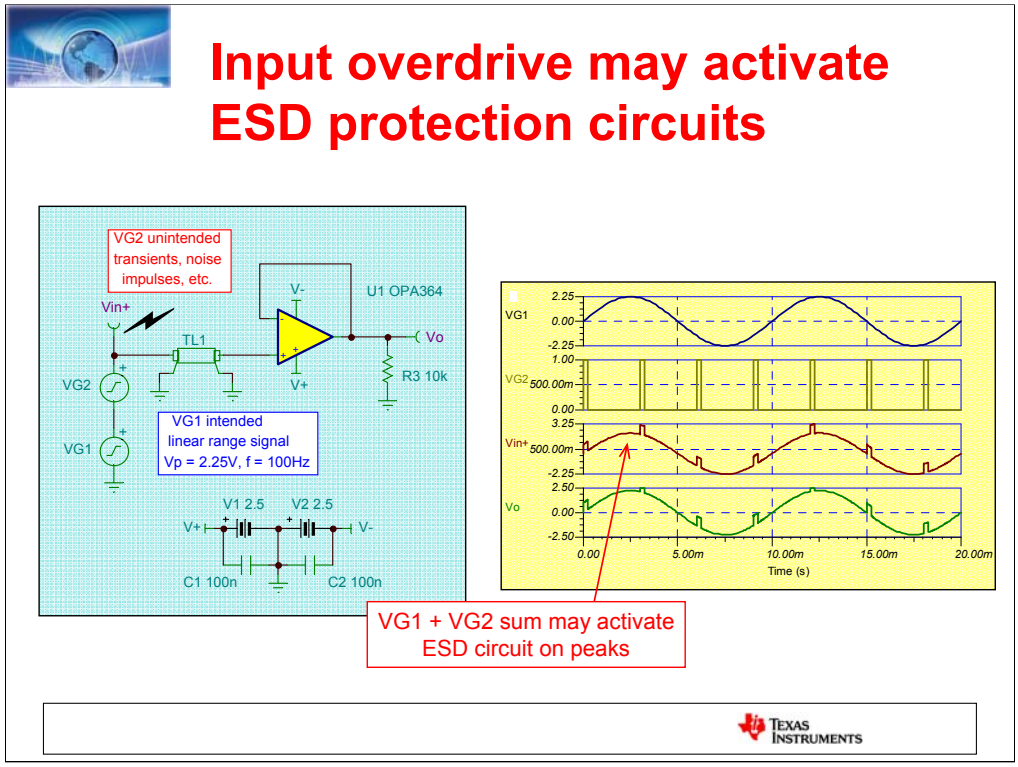
Texas Instruments

Sections of the INA168 die layout are shown depicting the various ESD protection structures. The input diodes are structures ESD1 and ESD2. ESD1 is the input-to-positive supply diode consisting of NPN base-emitter. ESD2 is the input-to-negative supply diode comprised of an N-sinker and buried-layer to substrate structure. ESD7 and ESD8 are comparable to ESD1 and ESD2, respectively, but connected at the output pad.

The third section is that of supply clamp device consisting of a large NPN transistor. This device is slated to conduct during an ESD event, clamping the supply-to-supply voltage and absorbing and releasing the energy associated with the event.



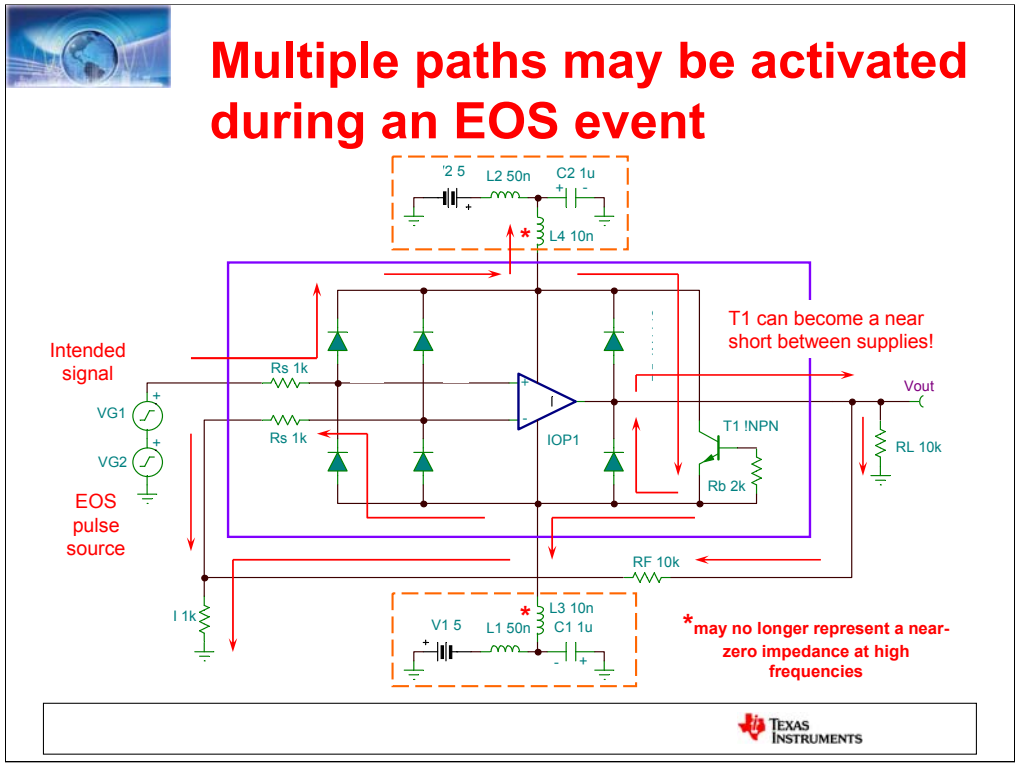
This example shows possible current paths to ground during an ESD discharge event. An ESD event most often takes place between 2 pins; one floating and the other at a much lower potential such as ground. Several paths exist here; from an input, through an ESD protection structure to ground.



This is an example of a simple follower circuit comprised of a low power, OPA364, CMOS op-amp. The intended, low frequency signal represented by VG1 is the desired transducer output.

If the transducer is located a distance from the amplifier and they are interconnected by cables, twisted pair wires or other lines, noise and/or transients can be induced from the surrounding environment. Transients may also be an artifact of the transducer connected to the amplifier.

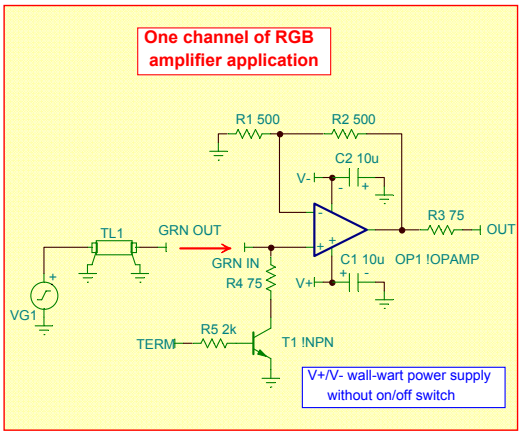
VG2 illustrates an unintended transient source that is simply added, or rides upon the intended transducer output signal. The summed signal amplitude is sufficient to exceed the maximum specified input range for the amplifier. If sufficiently large, the ESD circuit may be triggered by the input signal.

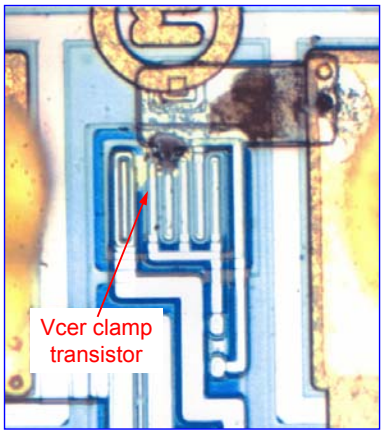


The current path created by an EOS event can be complex and somewhat unpredictable; more so at high frequencies where stray impedances become significant. The normally near-zero impedance power supply paths, which may be such at DC, may exhibit significant reactance at high frequencies.

A main consideration is that any of the paths through the device can safely withstand the current and voltages present during the event – while protecting the analog circuit. If they are incapable of doing so, they, or the analog circuit may be damaged due to the joule heating that takes place as the power is dissipated.

Clamp transistor failure due to an EOS/ESD event



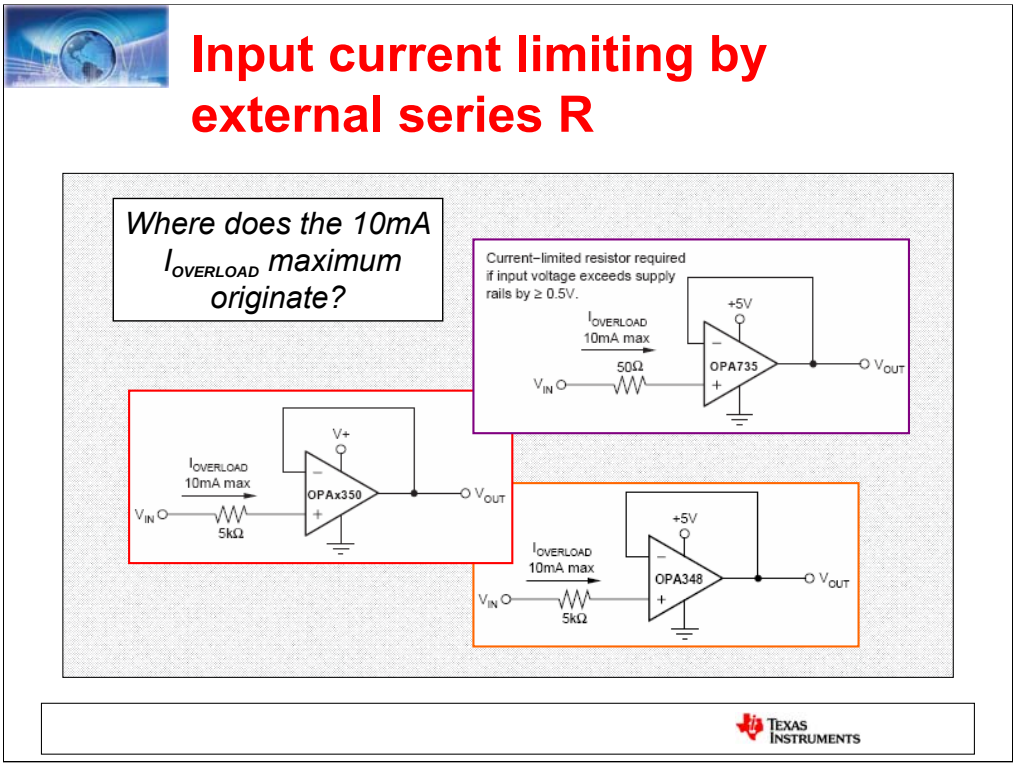


This is an actual application of a high-speed op-amp where the ESD clamp transistor was damaged by an EOS event. This problem was repeatable and devices could readily be damaged when a charged cable was connected to the BNC connector at the op-amp's non-inverting input.

There were two conditions that would set the clamp transistor up for failure; 1) The circuit was powered by a "wall-wart" that didn't have a on/off switch, 2) T1, the input termination switch, was not initially engaged, rendering the op-amp input in a floating state.

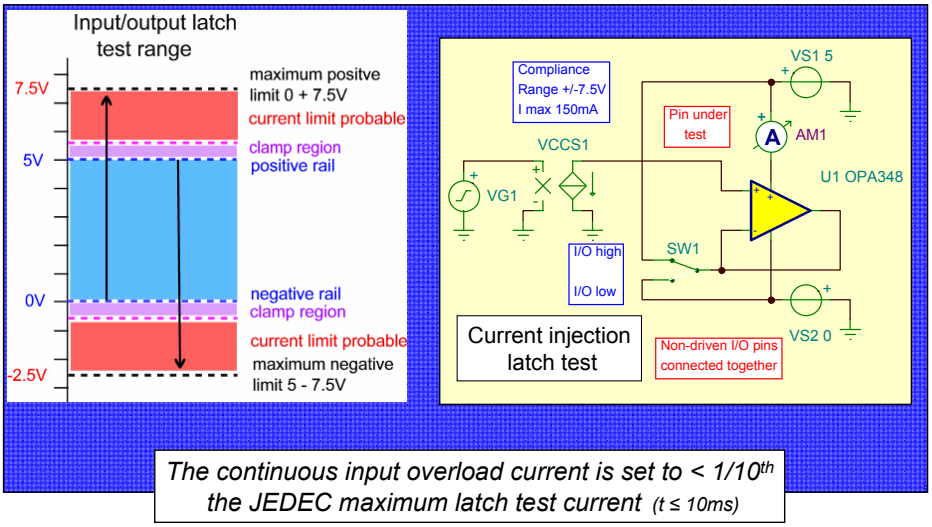
When a charged cable was connected to the input of the powered circuit, the EOS pulse would raise the supply rails to the point where the clamp transistor, T1, went into a BVcer condition and conducted. Because the supplies were continuously "on" T1 appeared as a near short between the supplies.

T1's safe operating conditions were quickly exceeded resulting in extreme joule heating, melt down and destruction.



A review of the TI-Tucson CMOS op-amp data sheets will yield numerous models recommend adding an input protection resistor to circuits where an over voltage might occur. This resistor is added to the circuit to limit the input current to a safe level. This current is referred to as $I_{OVERLOAD}$ and is the maximum continuous value the input circuitry can withstand without sustaining damage. The limit is established at 10mA. But where does this value come from?

Parasitic circuit latch testing



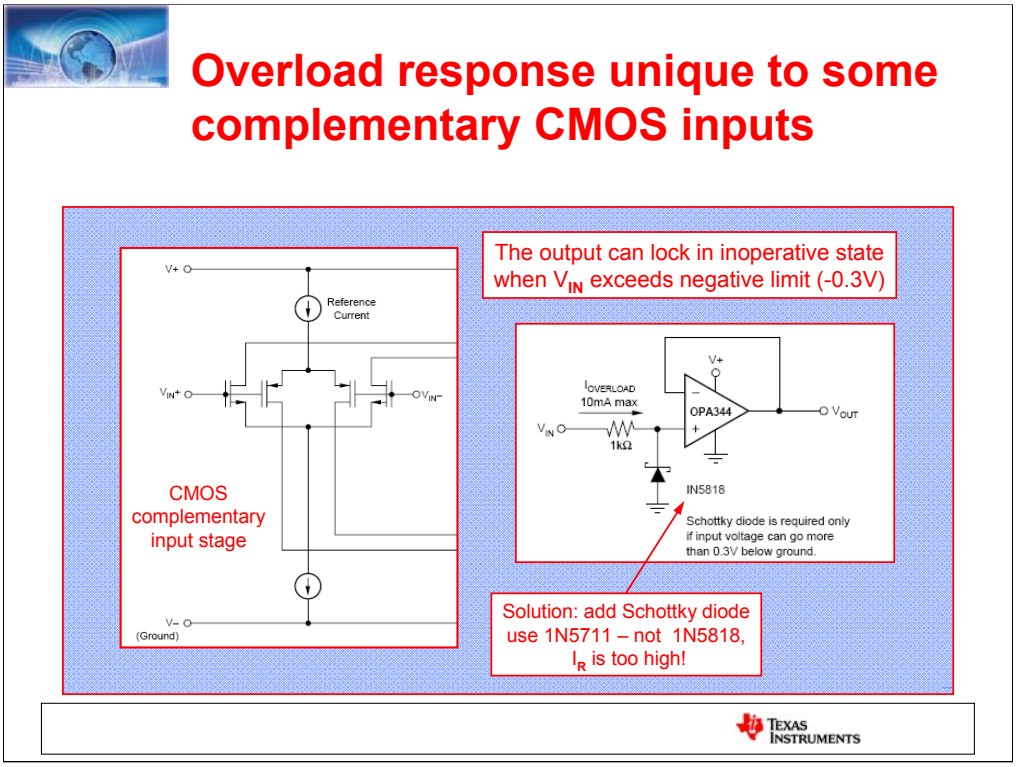
Latch testing of analog integrated circuits is a normal qualification requirement. The purpose is to identify parasitic semiconductor structures that may latch “on” when the input, output and power supplies pins are subjected to voltage impulses. Latched parasitic devices may lead to abnormal circuit operation or even destructive current paths.

One requirement of the latch test series is the Current Injection Test. During this test a particular I/O pin is subjected to a voltage pulse that is equivalent to the full, supply-to-supply voltage; 7.5V for the OPA348 example. The supplies pins are set to the nominal supply voltage and all other I/O pins are connected together at one supply rail voltage, then at the other. The pulse duration is less than 10ms. The current is limited to 150mA and should this value be reached the pulse voltage ceases to increase any further.

This sequence is conducted with the I/O voltage swept from the lower power supply rail voltage (0V) to the maximum positive voltage (7.5V) and from the upper supply rail voltage (5V) to the maximum negative voltage (-2.5V).

Once latch testing is completed the device is electrically tested. This is to establish whether the device remained undamaged, was impaired or electrically damaged.

As mentioned the input current is limited to 150mA. The ESD clamp diodes nearly always conduct first and limit the pulse voltage when it exceeds the rail voltage by about 0.6V. HPL Design Engineering has established that if the device survives the 150mA pulse event that the internal devices can safely withstand a maximum continuous current of 1/15th this value - 10mA.



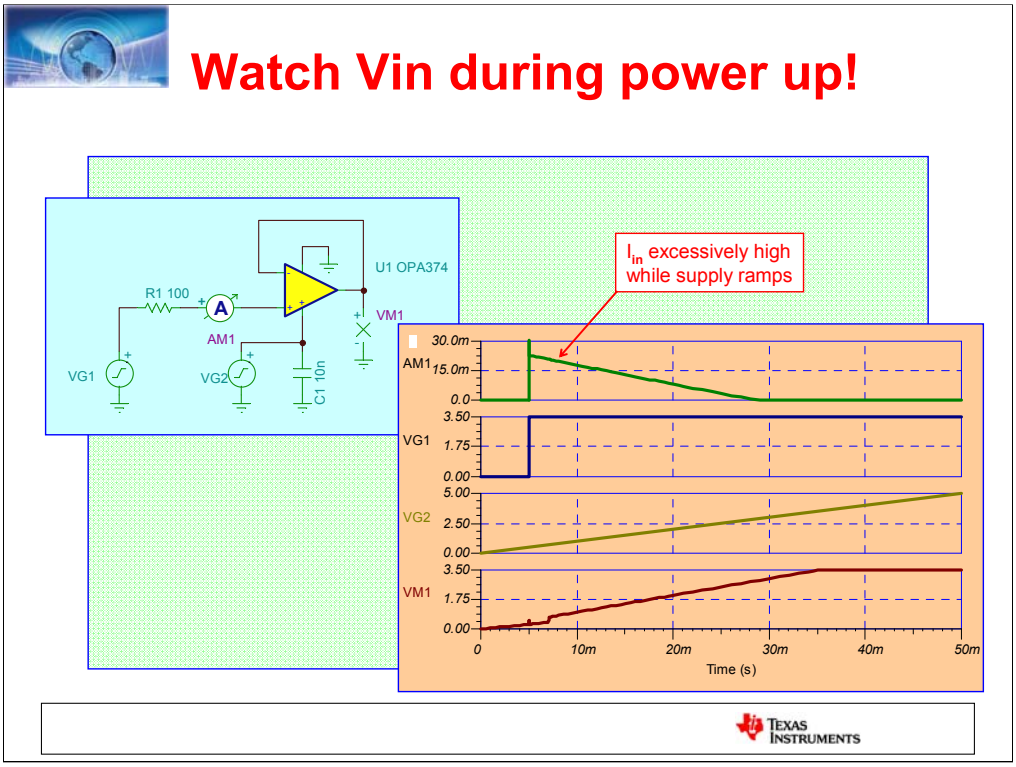
Some rail-to-rail input op-amps utilize complementary N and P channel differential input pairs to achieve input voltage operation to, or below the supply rails. Where one input pair may be biased off by an input voltage excursion close to the opposite rail, the other input remains biased and continues to operate within its linear CMV range.

For the OPA344 example shown, it has a CMV range 0.3V beyond the supply rails. Using nominal supply rails of 0 and +5V the CMV input range is -0.3 to +5.3V. Normal ESD clamps and series current limiting would protect the inputs beyond this range.

One unique characteristic of this device is revealed when the input voltage is taken more than 0.3V beyond the negative rail. In this particular case, the op-amp may lock up in an inoperative state. Normal operation can be re-attained by removing the negative input overload and cycling the supply back to zero and back to full.

That isn't always convenient and a more automatic solution is to include a small-signal, Schottky diode from the input to the negative rail. The diode's forward turn-on voltage is about 0.3V at 1ma.

One drawback to this protection approach is the Schottky diode can have significant reverse leakage (I_R) current while being reverse biased within the op-amp's normal CMV range. Considering the OPA344 has a maximum I_B of ±10pA at 25c, the 1N5711 may have leakage current closer 10 to 100nA at the same temperature. That is orders of magnitude higher than the input current. But note, the I_R for 1N5818 shown in the PDS can be closer to 500uA at room temperature!



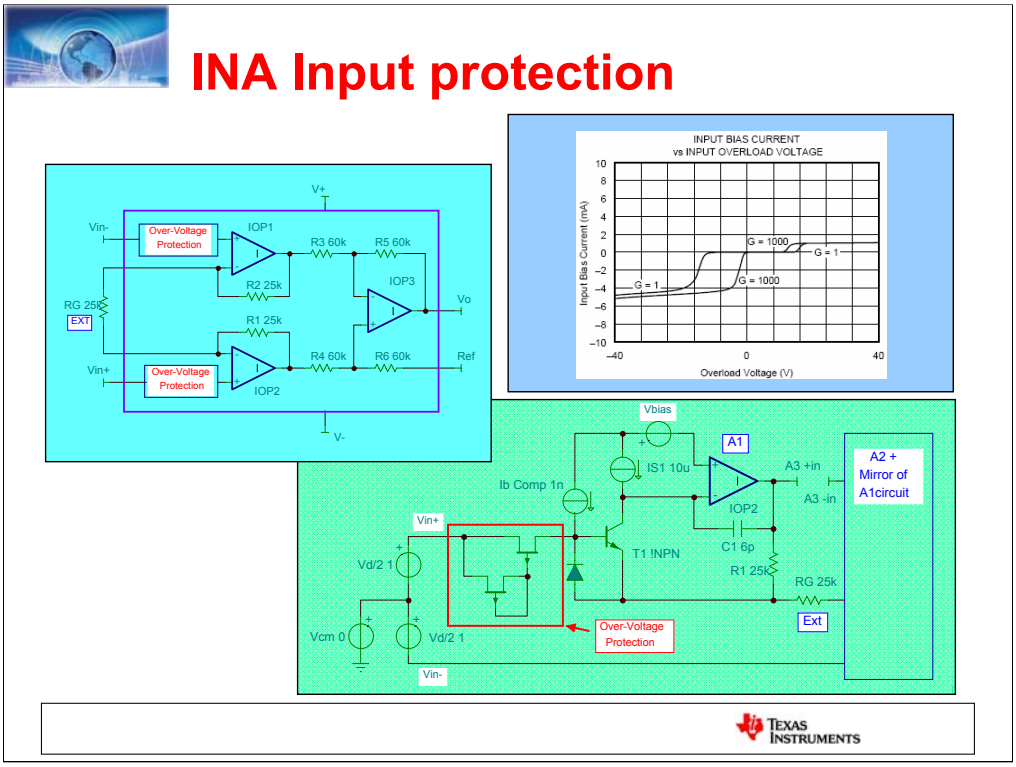
There are applications where the input signal is present before the power supply voltage is applied to the amplifier. Such a scenario has the potential to damage the input ESD protection circuit if the current is limited to a safe value.

For illustrative purposes the supply is slowly ramped from 0V to 5V in 50ms, while the 3.5V input signal is applied just 5ms after the supply begins its ramp.

The problem with this scenario is the inputs are initially higher than the positive rail voltage, which turns on the positive ESD diode. This continues until the voltage difference between the supply and input is somewhat less than 0.6V.

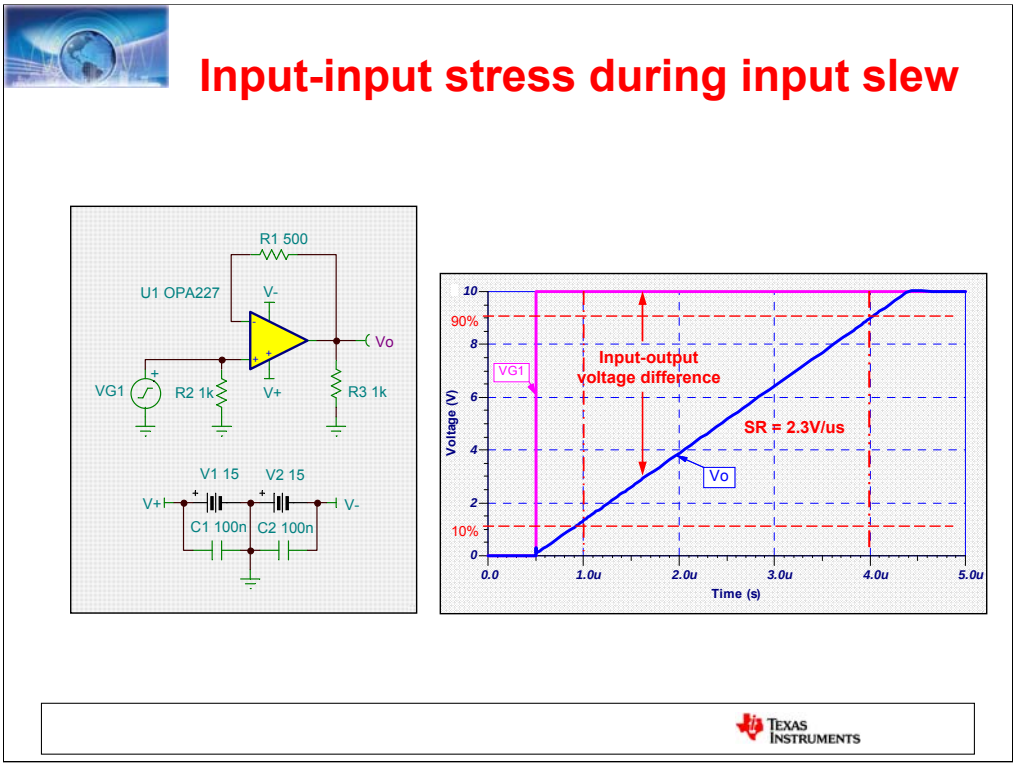
If the input source has a low impedance and can deliver the current and there isn't a source limiting the current, then a potentially harmful current could flow through the ESD diode.

Again, including the series input resistor will protect the input circuit from such damage.



The INA116, INA118 and some of the other 3-opamp instrumentation amplifiers have a JFET current limiting circuit in series with the inputs. This circuit protects the input from voltages as high as +/-40V. When the instrumentation amplifier is operated within the normal linear input range the JFET circuit appears as a low resistance in which the base or gate current flows.

When a large voltage, outside the linear range is applied to the input, the current through the JFET will increase but to a safe limit dictated by the FET “ON” characteristics. The internal ESD input diodes route the current to the supply rails.

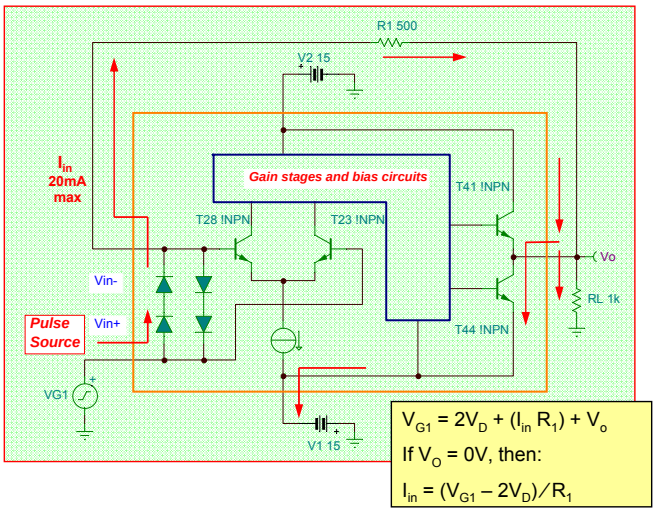


Another not-so-obvious, but potentially damaging, situation arises when an amplifier input is subjected to a large signal, fast-edged pulse. In this case a 10V peak rectangular pulse. The amplifier responds to the pulse by producing a linearly ramping output voltage whose characteristics are dictated by the amplifier's limited slewing-rate, in this case about 2V/us.

During the slewing time, the time required for the output to reach the input pulse's peak value, a large input to output voltage differential exists. Initially that value is 10V for the above example, but decreases after slewing is complete. Meanwhile the op-amp internal circuitry and feedback elements must handle that the current that flows during this period.

Often, internal protection circuits are added to the input circuitry to prevent damage to the op-amp's input stage.

OPA277 input-to-input slew rate protection



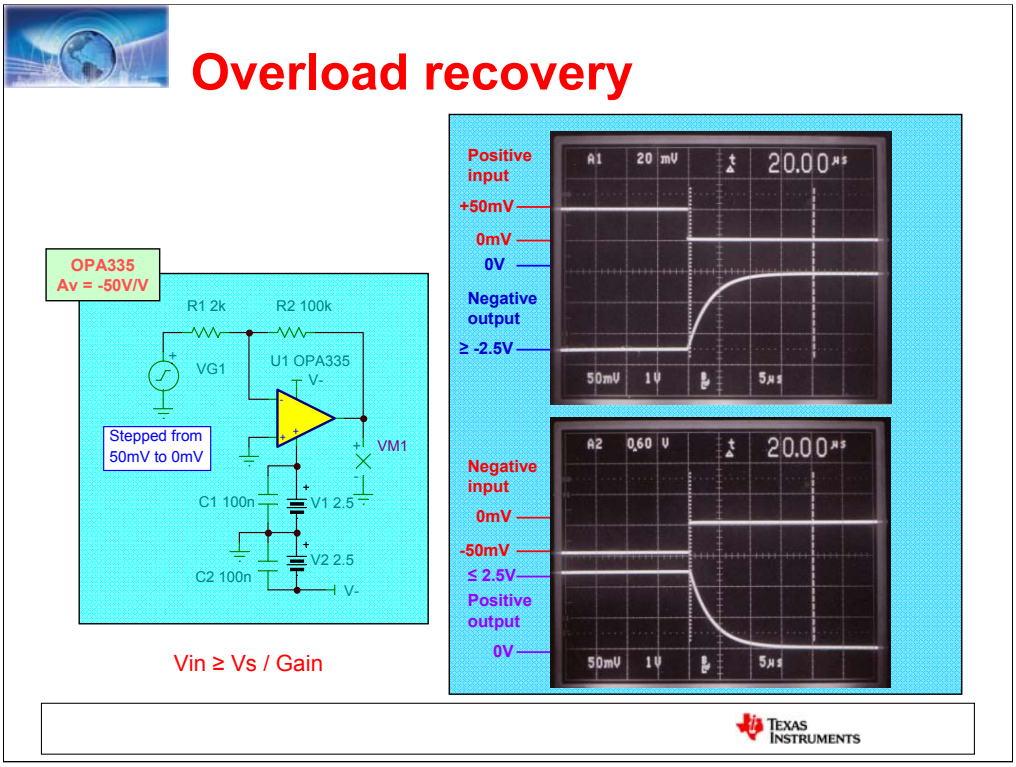
Texas Instruments

This simplified OPA277 schematic shows the slew-rate protection circuit employed at the amplifier's input. Two series diodes are connected between the bases of the differential input devices, T28 and T23.

For the moment, imagine that the series diodes are removed from the circuit. Unless a sufficiently large voltage is applied only the input bias current will flow into the input. However, if the applied voltage is large enough it will overcome the emitter-base forward voltage drop of T23 and the base-emitter reverse breakdown voltage [$V_{(BV)EBO}$] of T28. Current would then have a path to flow via the feedback path to the output.

Exceeding the reverse breakdown of a transistor's emitter-base junction has irreversible, detrimental affects on the transistor's electrical characteristics which in turn degrades the op-amp's input characteristics.

Including the series diodes clamps the base-to-base voltage at roughly 1.4V, and prevents the transistors from ever going into the reverse breakdown condition. The diodes then carry the current associated with the pulse while the amplifier slewing takes place.



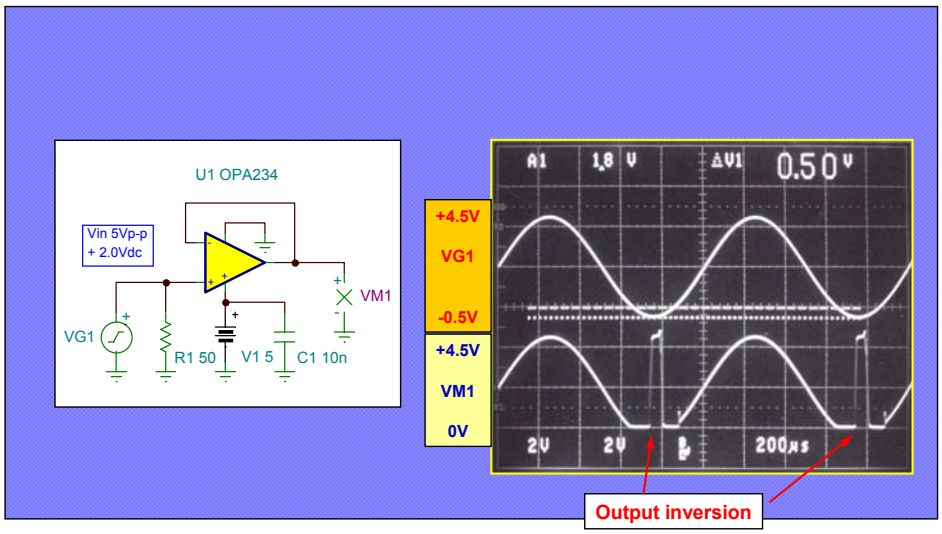
A-to-D converters have been tested for overload recovery for years to assure that the digital output does not change to an unusual code condition when the input is overdriven. This test also provides the time required by the converter to recover once the input overdrive condition is removed. Similar testing is being applied to auto-zero,CMOS op-amps to assure that they do not misbehave during an overdrive event or after it has ceased.

The overload recovery test is conducted with a small signal input and a high gain such as -50V/V. This is to avoid slew rate limiting in the input stage. The input level is initially set to a level near or beyond the end of the CMV range, but not so high has as to begin turn on of the ESD protection circuit. Either the input, output, or both may be driven into their respective rails during the overload period. Both positive and negative overload conditions are tested.

The input voltage is stepped such that the output moves off the rail to 0V. The time required for the output to achieve 0v (± offset) is the recovery time. For the OPA335 rail-to-rail amplifier shown this is about 20us. This measured result closely coincides with the plots shown in the data sheet.

One may be inclined to think that because this is an inverting circuit that the summing junction will always be very close to 0V. But that is only the case for an ideal op-amp. The summing junction of the non-ideal op-amp will momentarily follow the input source because of its internal delays and subsequent finite response time.

Output inversion during input overdrive

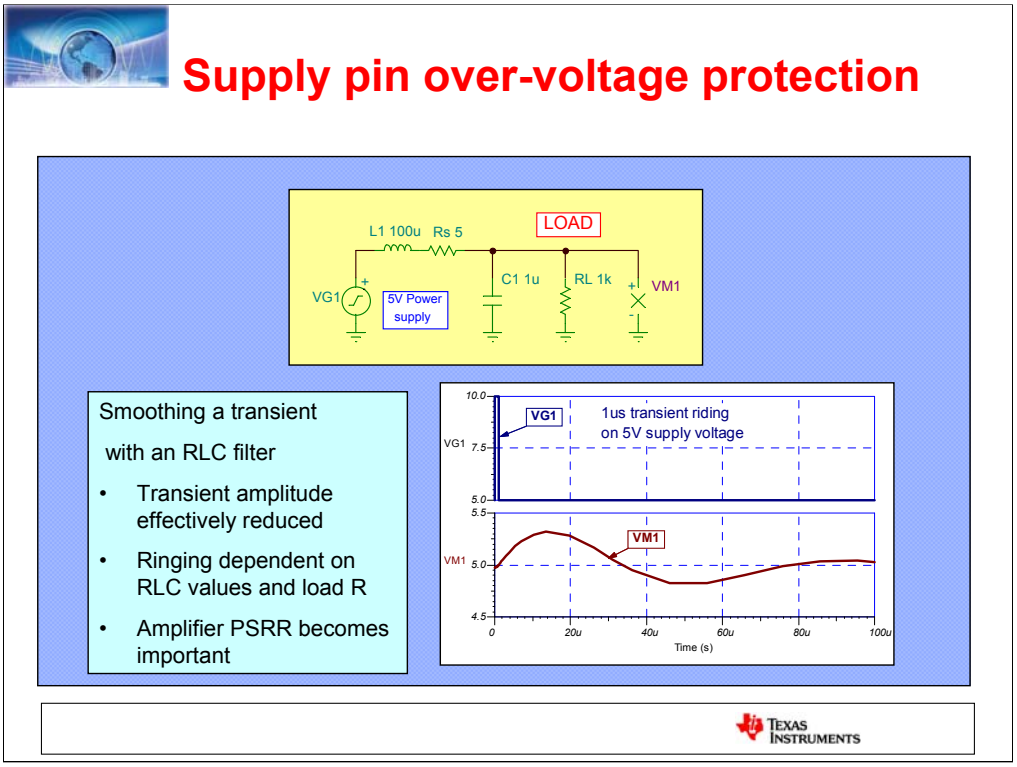


Some operational amplifier models exhibit an output inversion characteristic that accompanies an input overdrive. Most op-amps models do not exhibit this characteristic, but when one does precautions should be taken to prevent the input from being overdriven to the output inversion point.

For the example shown the input is being driven about 0.5V below the negative supply rail. The output level inverts momentarily from the negative rail to the positive rail. The duration of the output inversion worsens the more the input is overdriven. Obviously this is an undesirable condition that can have destructive consequences if the load is electromechanical in nature; a motor, actuator, etc.

This particular example circuit can be remedied by placing a reverse-biased Schottky diode between the non-inverting input and negative supply rail.

Output inversion was covered extensively in the 2005 AFA deep dive conference. For more information refer to the conference proceedings.



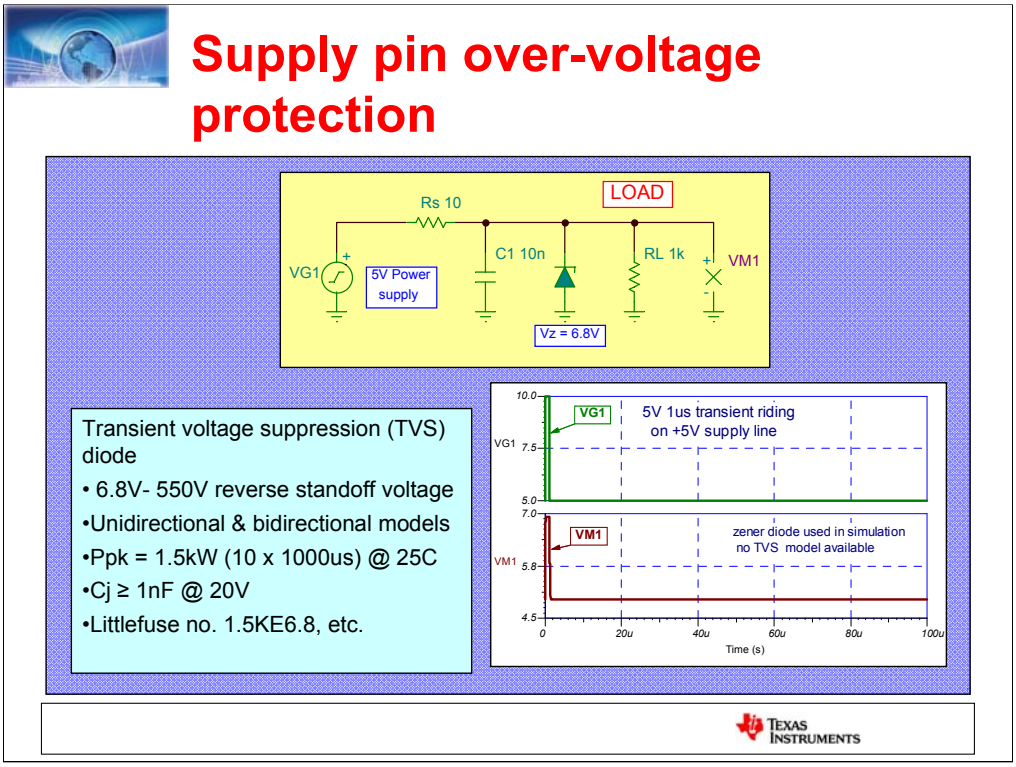
A switching power supply may be corrupted with high-frequency transient energy. This is especially true for switching power supplies that use high-frequency MOSFETs to perform the switching function. The voltage “spikes” provide the potential for an over voltage condition across the amplifier’s power supply pins. Should the supply voltage exceed the voltage breakdown of the internal circuits a direct current path can be created between the supply pins, leading the device failure.

Protecting the device from a power supply transient can be accomplished with an RC or RLC circuit. This may be done unknowingly by a common on-board EMI/RFI filter. However, the circuit’s response can vary tremendously depending on the RLC constants and the load characteristics.

The simple RLC circuit is connected to a load resistance in the accompanying slide. The +5V supply has a 5V, 1us transient imposed upon it, equivalent to a 10V spike. This well exceeds the maximum supply voltage for most low voltage CMOS processes. The 1K load resistance simulates an amplifier drawing a supply current of about 5mA.

It can be seen from the response that the RLC circuit integrates the spike into a sinusoidal response riding on the +5Vdc level. The slight over voltage should not pose a problem for the device.

Besides the unknowns associated with the RLC circuit combination in many cases, the supply voltage does undershoot. This will affect the op-amp output offset. The op-amp’s PSRR will help minimize the change in the output offset, but it is a notable error.



A better, more predictable transient suppression method is to use a Transient Voltage Suppressor (TVS) on the supply line. It is similar to a zener diode, but is specifically designed to withstand very large transient current and peak power.

The Littlefuse 1.5KE series of TVRs is available with a reverse standoff voltage from 6.8V to 550V, in both unidirectional and bidirectional polarities. The peak power P_{PK} capability is 1500W, for ten 100us pulses.

An obvious advantage is the fast voltage clamping characteristic with no undershoot of the supply voltage.

The model and response shown in the slide are actually for a zener diode as no TVR models exist in TINA. However, the response should be quite similar to that shown.

Supply pin over-voltage protection

Surface Mount Varistors

Multilayer Transient Voltage Surge Suppressors

RoHS Pb ML Varistor Series

Littelfuse

Features

- Multilayer ceramic construction
- Operating voltage range $V_{M(DC)}$ = 5.5 to 120V
- Rated for surge current (8 x 20us)
- Rated for energy (10 x 1000us)
- response time <1ns for zinc oxide
- Inherent bidirectional clamping

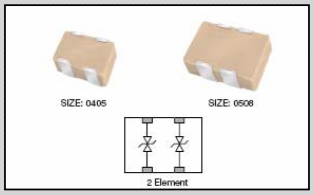
Texas Instruments

An alternative to the zener type TVS is the varistor. It is similar to the conventional junction type varistors except it utilizes ceramic technology based semiconductor materials. One example is a zinc oxide varistor.

They have advantages compared to the conventional zener in that the TVS operates over a wider temperature range with a flatter voltage vs. temperature response and provides inherent bidirectional clamping. They are available in relatively low capacitance (<100pF) versions and with very fast response times (<1ns).

Externally connected input protection devices

Transient voltage suppressors
For CMOS, bipolar and SiGe



Features:

Available from 5.6 to 18V

DC working voltage ≤ 18V

AC working voltage ≤ 14V

Turn-on-time <1ns

Repetitive spike capability

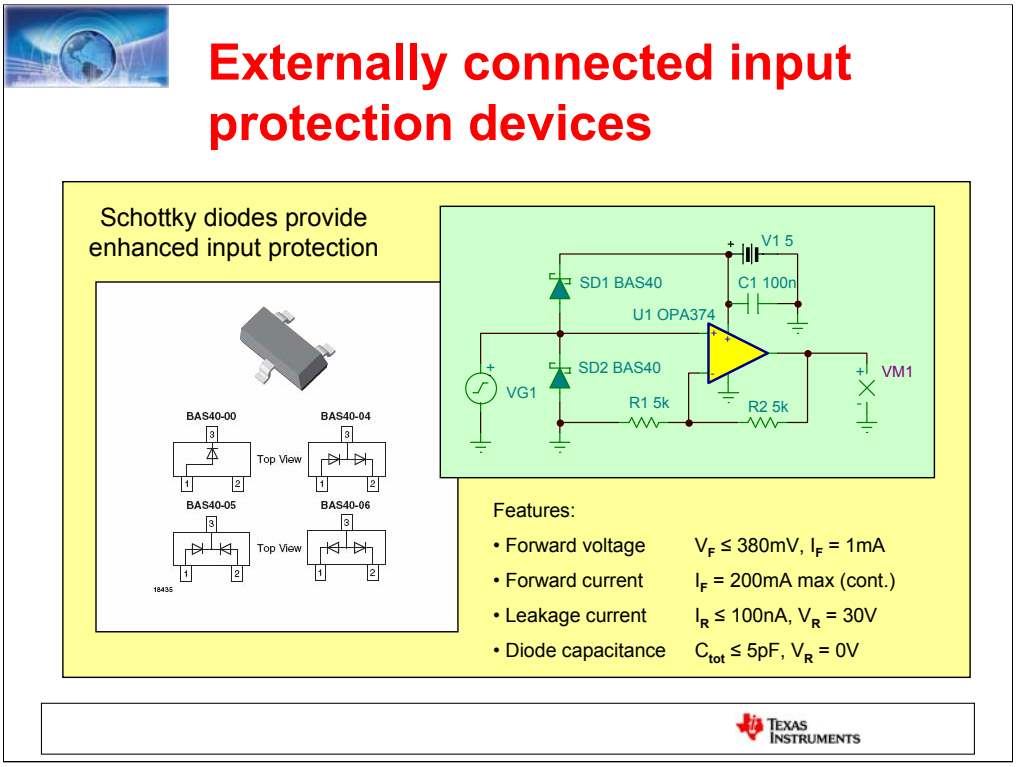
ELECTRICAL CHARACTERISTICS PER ELEMENT

							uA	J	A	pF
	AVX Part Number	Working Voltage (DC)	Working Voltage (AC)	Breakdown Voltage	Clamping Voltage	Test Current For V_c	Maximum Leakage Current	Transient Energy Rating	Peak Current Rating	Typical Cap
2 Element 0405 Chip	MG042S05X150 _ _	5.6	4.0	8.5±20%	18	1	35	0.05	15	300
	MG042L14V400 _ _	14.0	10.0	18.5±12%	32	1	15	0.02	15	45
	MG042L18V500 _ _	18.0	14.0	N/A	50	1	10	0.02	15	40

Texas Instruments

Here is another type of Transient Voltage Suppressor that is intended for input protection. The device can be selected such that the breakdown voltage is just a few volts above the input operating voltage.

Any protection device attached to the input of an analog IC must be understood relative to the application. Such devices can degrade the overall circuit performance either from a DC, AC or both stand points. However, if the circuit can tolerate the leakage current, added capacitance or other parametric degradation then these added devices can offer an increased level of EOS protection.



The Schottky diode has a lower forward voltage than a similarly rated silicon junction diode at a given current level. For instance, the small-signal Schottky diode will have a forward voltage closer to 250 to 300mV at 1mA, compared to something on the order of 550 to 650mV for the junction diode operating at the same forward current.

When Schottky diodes are placed from the amplifier input to the supply rails, they shunt the internal junction diodes. They turn on earlier than the internal diodes and will carry the majority of current during an overload condition.

The internal ESD diodes may only be rated 10mA continuous, whereas, the external Schottky diodes are rated at 200mA continuous current (TA = 25°C).

Summary

- EOS and ESD events may activate ESD protection but result in different outcomes
- Internal ESD circuits may sufficiently handle EOS
- Be aware of unique EOS situations such as power up and input slewing
- External EOS protection circuits may be required if device damage is probable