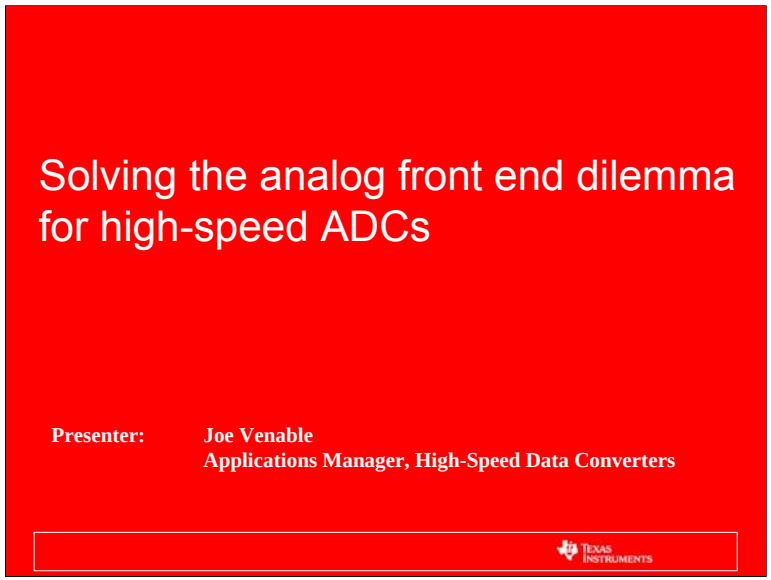


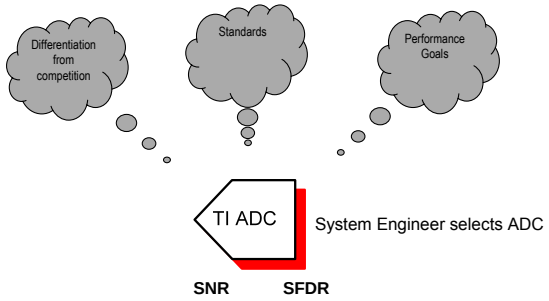
This presentation combines the efforts of several different groups and presentations.

This particular issue is quite difficult and very confusing due to many different variables and some misunderstandings.

We will try to set up of method for analysis, some useful approaches, and reported results here.

Topics

- High-Speed A/D Converter Testing & Performance Metrics.
  - Test circuits used to generate HS-ADC data sheet plots
  - Definitions
- Combining SNR and SFDR for ADC + Amp + Input Signal
  - Circuit and System-level models
- Survey of Amplifier Topologies Used in ADC Interfaces
  - Real-life application circuits
- Combined amplifier/ADC EVM
  - TSW1070



After the ADC selection is made, how do you design the interface circuit to not degrade performance?

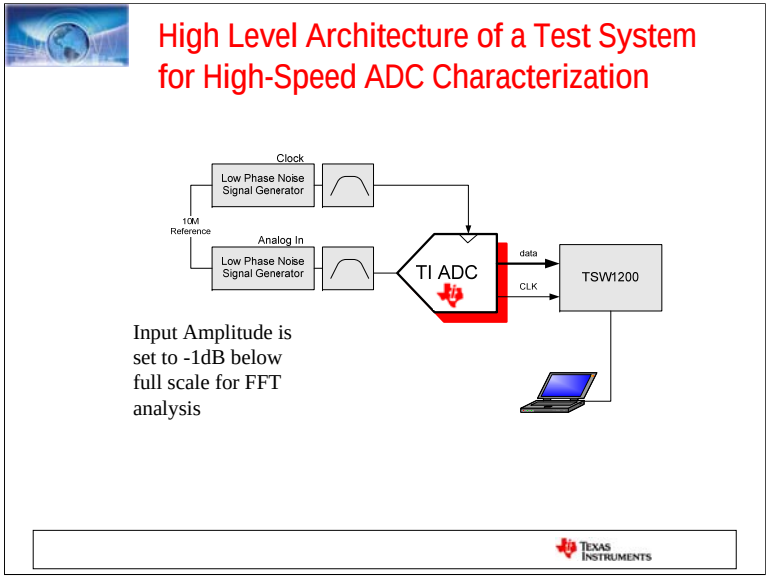
Goal #1: Design an interface circuit to achieve the ADC's SNR.

Goal #2: Design an interface circuit to achieve the ADC's SFDR.

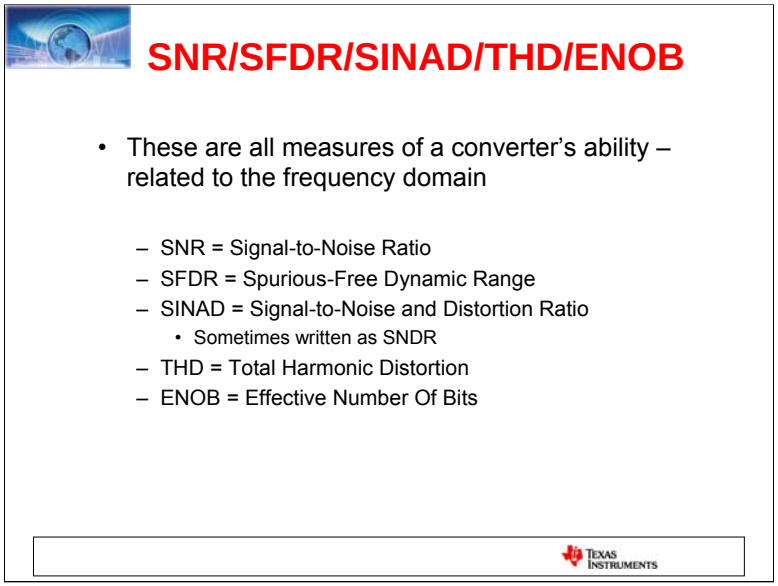
High-speed data converter testing, metrics

Interface circuits and performance metrics used in the characterization of High-Speed ADCs

Texas Instruments

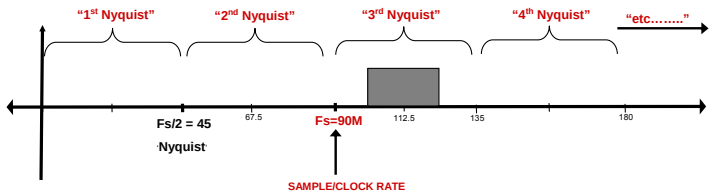


Very controlled characterization environment for the converters. Key element is the 8pole passive bandpass that strips away almost everything but the desired single tone for FFT testing.



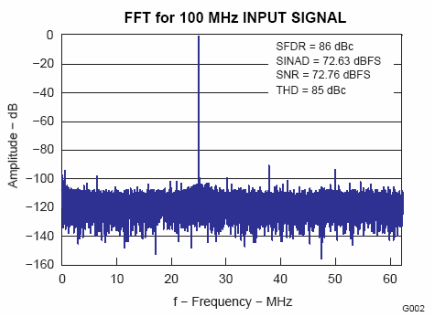
ENOB = (SINAD – 1.76)/6.02

Nyquist Zones



Typical Output Spectrum from ADC Lab Testing

ADS6445
125MSPS clock
100MHz input



- All observable spurs and most of the noise is generated by the ADC in this test.
- Slight increase in the noise floor near the test signal is due to the signal source.
  - Band-pass filter allows noise to enter the system from the RF signal generator.
- All broadband noise folded is aliased into the 1st Nyquist zone.

Active HS-ADC Interface

Amplifier performance metrics in the time-domain

Combining SNR and SFDR for ADC + Amp + Input Signal

Circuit and System-level models to help pick the best driver amp

- Validation using the TSW1070 EVM

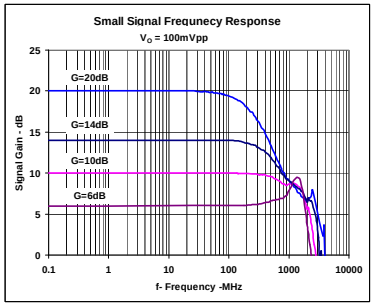
Bandwidth

- Small signal bandwidth is related to small signal rise and fall times

$$\tau \approx \frac{0.35}{f_{-3\,dB}}$$

- f_{-3dB} is the -3dB corner of the small signal response.

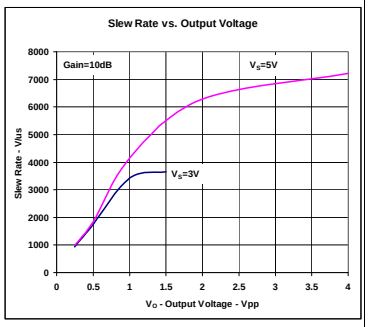
SS Frequency Response
Shown in data sheet
Depends on Gain in VFA
Important for Stability Analysis



Slew Rate

[depends on signal level]

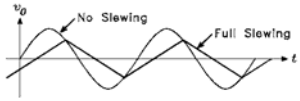
- Slew Rate defined as the maximum $\Delta V/\Delta t$ for a specified gain, output level and R_{LOAD}.
- Key parameter in some continuous-time systems.
- System requirements may be dependent upon front-end processing in sampled-data systems.
  - Front-end filters
  - Anti-aliasing filters
- Slew Rate limits large signal bandwidth



Texas Instruments

Slew Rate: Sine Wave Input

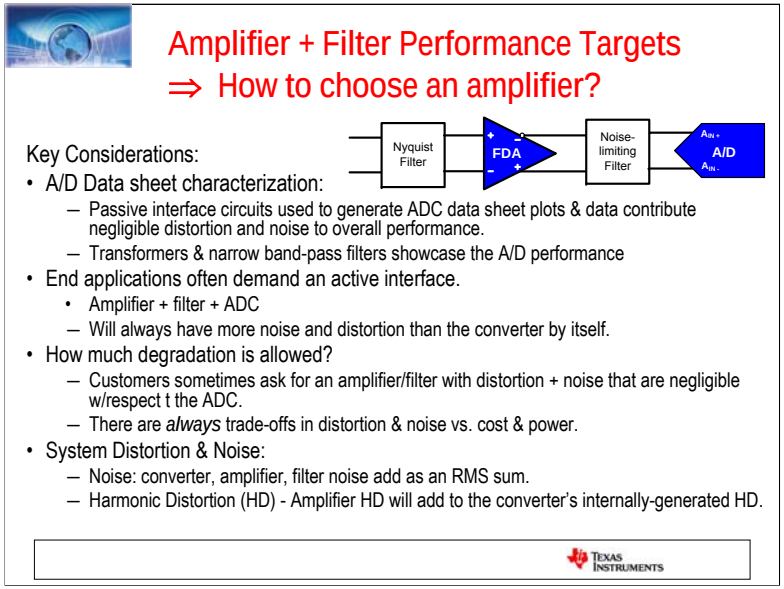
- When an output sine wave is driven into full slewing, it becomes a **triangle wave**
- The **slew-limited peak** is given by the slope multiplied by ¼ the period
- When the op amp is driven into **full slewing**, an increase in the amplitude of the input signal causes no change in the output amplitude.
- **Slew Rate Limiting:** Distortion in the output signal caused by the slew rate of the device being too slow to allow the device to respond properly to a change in the input signal.
- **Slew Rate** is not related to small signal rise and fall times.



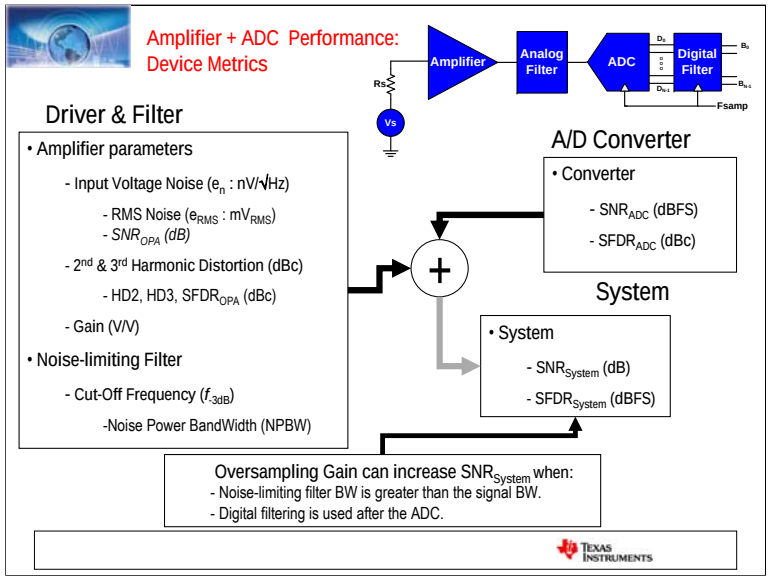
$$V_{Pslew} = SR \cdot \frac{T}{4} = \frac{SR}{4f}$$

Maximum frequency with no slew rate limiting is given by:

$$f_{max} = \frac{SR\ \sqrt{2}}{2\pi V_P}$$



Getting a combined SFDR is very difficult – Over frequency the dominant converter term may change from 3rd to 4th to 5th, etc. Good designs for the amplifier interfaces will be dominated by the 3rd harmonic. If that does not line up with the converters worst harmonic, it will be difficult to accurately predict SFDR.



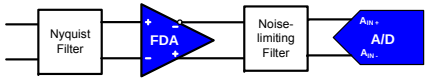
As shown above, amplifiers and converters are defined in different terms.
Amplifier noise is usually referred as spot noise in both current and voltage terms.

Combining the input voltage with the amplifier gain and the filter cut-off frequency, it is possible to derive a signal to noise ratio (SNR_{OPA}) for the amplifier.

In the same manner, using the 2nd and 3rd harmonic distortion, the dominant distortion terms for an amplifier, it is possible to derive an Spurious Free Dynamic Range ($SFDR_{OPA}$) for the amplifier.

Given these SNR_{OPA} and $SFDR_{OPA}$ numbers, it is possible to combine them with those of the converter and see a predicted combined performance or system performance. This combination will be done at the converter input pins.

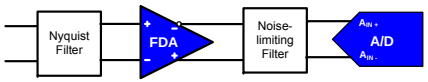
SNR & Noise Bandwidth



- Amplifier input
  - Assume an antialiasing filter before the amplifier input
    - This is not always true, especially in systems w/narrowband signals.
  - But use this assumption to design the last stage for limited degradation.
- Amplifier output
  - Assume amplifier output noise is white (flat spectrum),
    - Bandwidth-limited only by a noise-limiting filter.
  - Amplifier output noise voltage: $e_o = (P_N)^{1/2} = (N_O B_N)^{1/2}$ (V)

    where: N_O = Amplifier output noise density (W/Hz).
    B_N = Amplifier noise power bandwidth (Hz)
  - Rule of thumb: $BW_{AMP} > 5xBW_{SIGNAL}$ to minimize distortion.
    - Wide amplifier bandwidth is required for good SFDR performance.
- The noise power bandwidth of the amplifier/ADC interface is often neglected.
  - A low distortion amplifier solution needs bandwidth >> desired signal frequency.
  - Total noise power must be considered to avoid unpleasant surprises on SNR.

Noise limiting filter



- Unless a filter is used between amp and ADC, the ADC will integrate the amplifier's output noise up to the ADC's analog input bandwidth.
  - Broadband noise will fold into the first Nyquist band.
  - Analog Input Bandwidth could be quite large.
    Ex. AD5463=2GHz
  - Rule of Thumb: A simple first order RC lowpass filter will have 1.5x the noise as ideal brickwall filter.

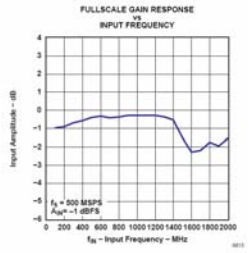
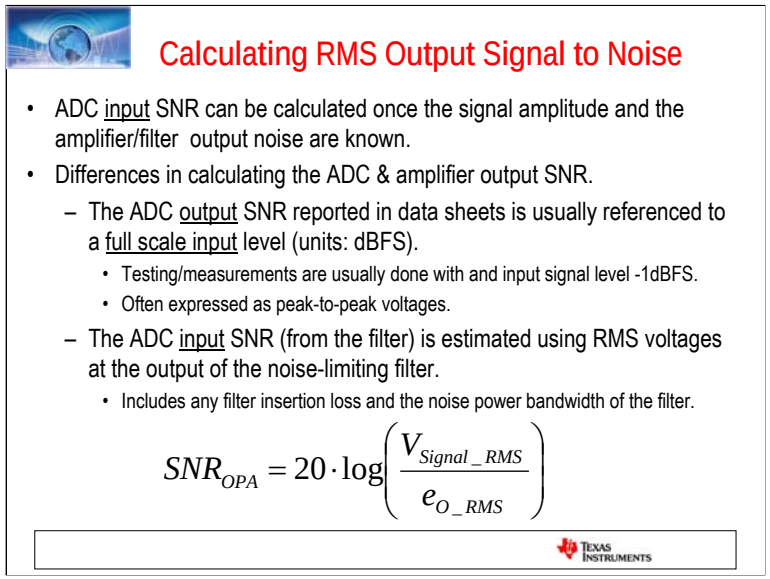


Figure 14.
ADS5463



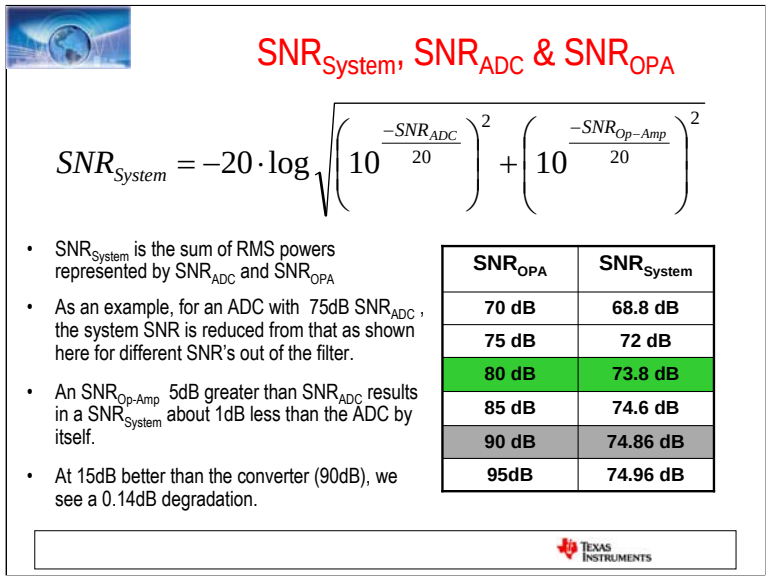
Finally we can calculate the SNR_{OPA} for the amplifier using the above SNR definition.

One difference in calculating the SNR for the converter and the amplifier.

The SNR is calculated at the input of the converter for the converter, thus using the full input range of the converter as defined in the datasheet.

For the Amplifier, the SNR needs to be calculated at the output of the Amplifier/Filter, thus using the full input range of the converter as value for the RMS signal.

All we have left to do now is to combine SNR_{OPA} with SNR_{ADC}

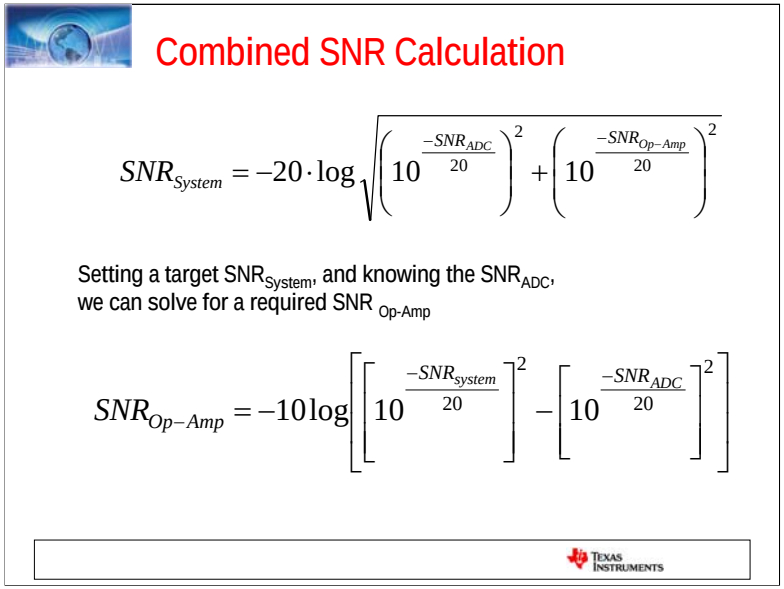


The SNR for the system is the RMS addition of SNR for the converter and the op-amp/filter combination. This implies that in order not to add too much noise in the amplifier stage, both filter and amplifier ought to have a very low noise. For example, with a 75dB SNR converter, in order to target a system SNR of 74.9dB, the SNR for the amplifier should be better than 85dB.

In amplifier terms, the SNR is the integrated output noise through a defined bandwidth. The bandwidth is limited by either:

•Post amplifier filter

•Amplifier small-signal bandwidth

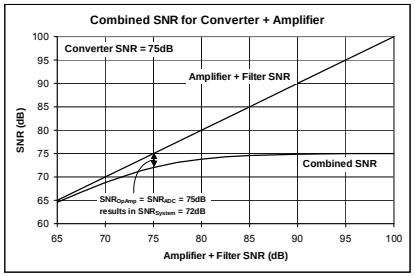


This equation can be solved easily for a required amplifier SNR to meet a System target SNR

This analysis is looking at arriving at a combined SNR at the converter input. This allows us to use the SNR of the converter and the broadband noise coming into the inputs, recognizing that the full integrated noise at the input will be folded into the 1st Nyquist zone in the FFT coming out of the converter.

Alternatively, the analysis could input refer the converter noise to some point earlier in the system, then look at input referred equivalent noise for the amplifiers.

Combined SNR with a 75dB Converter SNR



- The straight line is the amp & filter output SNR (same as the x-axis).
  - Combines with the ADC to produce the asymptotic curve of system SNR.
- Examples:
  - 0.4dB of degradation from SNR_{ADC}, requires an interface circuit with and SNR 10dB better than the ADC.
  - If the ADC & interface circuit have the same SNR, then $SNR_{System} = SNR_{ADC} – 3dB$.

Texas Instruments

As one would expect - if the ADC SNR and the SNR at the input are equal, you see a 3dB degradation in combined SNR.

Distortion: SFDR Degradation

- Points to consider when estimating the combined amp/filter & ADC distortion:
- Use a differential signal path for the driver amplifier and the ADC.
  - Critical to getting the highest system SFDR.
  - A symmetrical, differential signal path attenuates even-ordered distortion terms and leaves only 3rd order harmonics.
- No differential last stage amplifier?
  - A single ended amplifier will need to suppress even order terms.
  - Will demand increase power consumption.
- Consider a single tone ADC input…
  - The converter converts the input fundamental as well as the input harmonic distortion (from the interface circuit).
  - The ADC generates its own harmonics from the fundamental which combine with the input harmonics (with some phase angle).
- Lab tests have shown they appear to add coherently (in phase).
  - We can simply add voltages to get the total output distortion.

Combined SFDR Performance

$$SFDR_{System} = -20 \cdot \log\left(10^{\frac{-SFDR_{ADC}}{20}} + 10^{\frac{-SFDR_{Amp}}{20}}\right)$$

- **In a differential amplifier interface, distortion is typically limited in SFDR by the 3rd harmonic.**
- **If the converter SFDR is also limited by the 3rd harmonic, then they will combine in phase and give a net system SFDR given by the above equation.**
- **If the converter SFDR is limited by something other than the 3rd, then the data will need to be handled on a spur by spur basis and this calculation will NOT give the combined SFDR**
- **If the 3rd harmonics set the SFDR limit, the above equation can be solved for the required amplifier SFDR to get a desired system SFDR.**

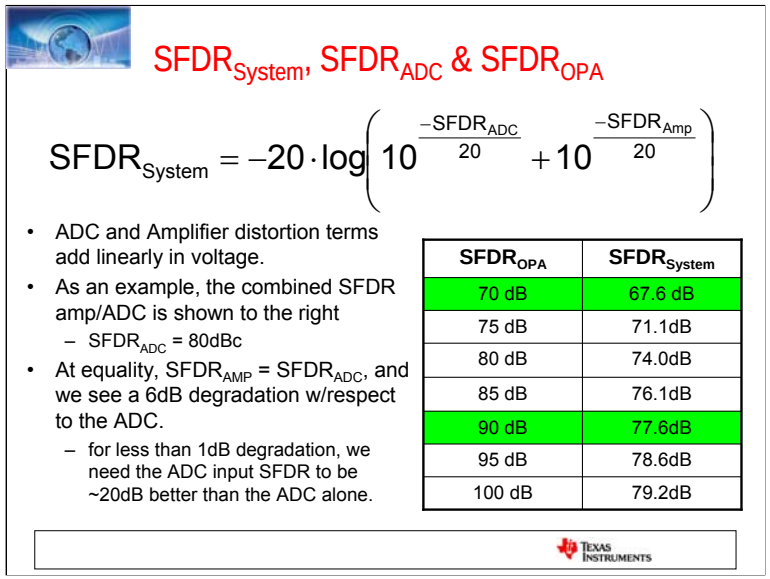
$$SFDR_{Op-Amp} = -20\log\left[10^{\frac{-SFDR_{system}}{20}} - 10^{\frac{-SFDR_{ADC}}{20}}\right]$$

Combined **SFDR Performance**

- In this calculation, we assume HD2 is attenuated by a symmetrical, differential signal path.
  - HD2 is negligible & we can consider SFDR is dominated by HD3.
  - If this is not the case, this calculation must be performed on a spur-by-spur basis.
- The first equation below shows the overall system SFDR and the second equation shows the required opamp SFDR.
  - Assumes system SFDR for the system and ADC are known.
  - Looks similar to the SNR calculation shown previously.

$$SFDR_{System} = -20 \cdot \log\left(10^{\frac{-SFDR_{ADC}}{20}} + 10^{\frac{-SFDR_{Amp}}{20}}\right)$$

$$SFDR_{Op-Amp} = -20\log\left[10^{\frac{-SFDR_{system}}{20}} - 10^{\frac{-SFDR_{ADC}}{20}}\right]$$

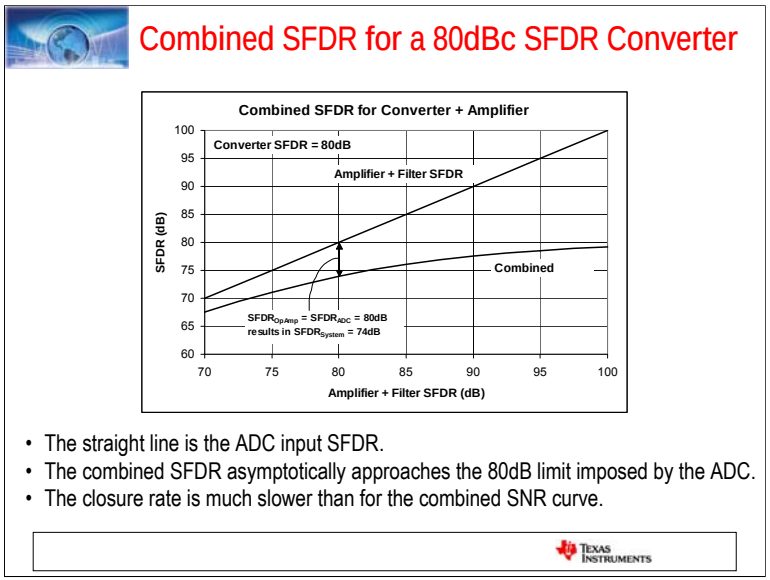


The SFDR$_{OPA}$ for an amplifier is given by the worst of the 2nd and 3rd harmonic distortion. Also the unit used for the amplifier is dBc or dB below carrier. For the converter, the SFDR$_{ADC}$ is expressed in dBFS or dB below Full-Scale. The method of matching these units is to extract the SFDR from the op-amp datasheet at the maximum input signal of the converter. For example, a 2Vpp full scale input for the converter ends up being 1Vpp for each output since the signal is differential.

Given that, the above equation shows that no matter how good the harmonic distortion of an given amplifier is, it will add in phase with the distortion generated by the converter, reducing the overall system performance. This result only applies when the worst amplifier harmonic is also the worst converter harmonic.

For example, a 70dBc converter SFDR is going to be reduce the system SFDR by 9dB if the amplifier distortion is 5dB worse than that of the converter (or 65dB). A 15dB margin between the converter and amplifier distortion will result in a system SFDR 1.5dB below the SFDR of the converter.

At low frequency, it is possible to find an amplifier for all converters. As frequency increases, this becomes harder if not impossible. Also, the amplifier should be operating at some gain in order to reduce the distortion requirement for the previous stages.



When the 3rd harmonics are adding in phase, we see a 6dB drop in combined SFDR performance when the SFDR coming into the converter is equal the converter performance.

To hold <2dB degradation, need to see > 12dB better SFDR coming into the converter.

To hold <1dB degradation, need to see >18dB better SFDR coming into the converter.

Some of the measured data appears to jump around quite a bit with input frequency and/or clock frequency - this is sometimes due to non-3rd harmonic terms being dominant in the converter SFDR. The differential stages tested here are 3rd harmonic dominated but the converters can have higher order dominant terms. If so, the theory here does not predict the SFDR correctly. It should simply be the converter SFDR in that case.

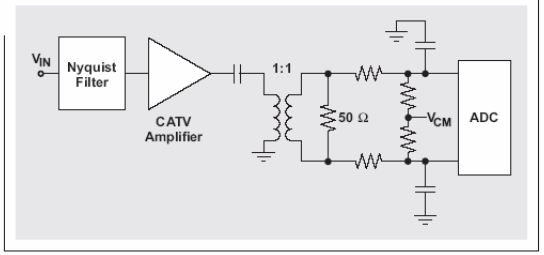
Survey of Amplifier Topologies Used in ADC Interfaces

Real-life application circuits

Texas Instruments

Topology#1: Single Ended RF amp drivers with last stage transformer interface

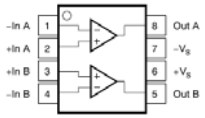
Figure 4. Single-ended amplifier driving a last-stage transformer



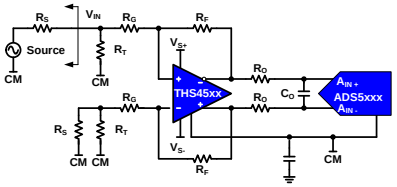
- Pros: Can have high performance at the expense of amplifier power consumption.
  - CATV amp shown above is often an RF amp.
- Cons: High quiescent power, size, AC Coupled only
  - The final-stage amplifier must produce very low even-order distortion.
  - Full-scale differential ADC input signal usually requires full amp output power.
  - Opamp-based drivers often provide a more efficient solution

High-Speed Op amps offer reduced power and cost for SE-Diff signal conversion

- Dual OpAmps
  - Single-ended input signal to differential output
  - With and without transformer.
  - Some of these circuits work pretty well,
    - Distortion can be limiting factor for fast signals
    - Suitable for 10 to 14bit systems.



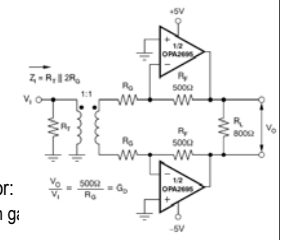
- Fully Differential Amplifiers (FDAs)
  - Easy & efficient way to provide DC-coupled single-to-differential conversion
    Independent common mode control



Some examples appear in the following slides.

Topology #2: Transformers for SE-Diff Conversion

- Best when used early in the signal chain followed by differential I/O stages.
  - Replaces this single ended I/O amplifier with a differential I/O structure as the final gain element
  - Reduces single-ended signal swing.
  - Very significant savings in HD2, power dissipation.



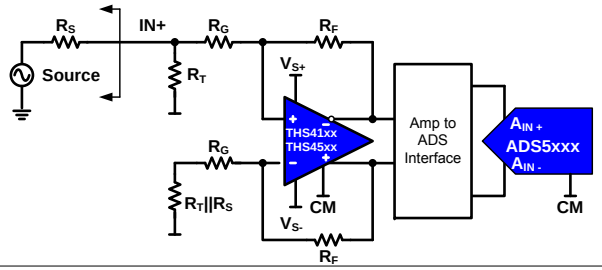
- Transformers can sometimes provide the best option for:
  - Low-distortion, low noise, AC-coupled applications when g
    not critical
  - But… be aware of frequency limitations.
  - Signal spectrum must not be near transformer band-edges.

Texas Instruments

OPA2695: Current feedback amps are useful for high gain and and high slew rate options.

Topology#3: FDA/ADC Driver for Single-to-Differential Conversion

- Basic circuit, SE input ⇒ Differential output
- Isolation circuit
  - Buffers amplifier output from ADC sample & hold switching.
  - LPF also reduces noise
  - BPF for narrowband signals
- Signal reference can affect device selection & the total parts count.

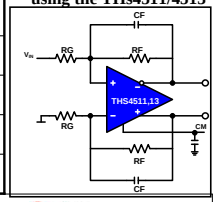


High-Speed FDAs

- High-speed devices
  - Low distortion, THD ≈ -75dBc @ 70MHz
  - Low noise, Vn ≈ 2 nV/√Hz
- Other features:.
  - Unity gain – THS4511, THS4513 can be used as unity gain buffers.
  - Single-ended supply - THS4508, THS4511
    - Enables ground-referenced sources with a minimum parts count.
    - Allows negative input signals while using single V_S = +5V.

Device	Min. Gain	Internal Level Shift?	Common Mode Range of Input (@Vs=5V)
THS4508	6 dB	Yes	–0.3V to 2.3V
THS4509	6 dB	No	0.75V to 4.25V
THS4511	0 dB	Yes	–0.3V to 2.3V
THS4513	0 dB	No	0.75V to 4.25V

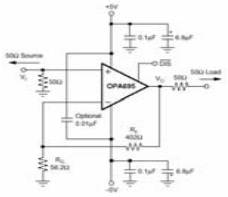
Example: LPF with gain using the THs4511/4513

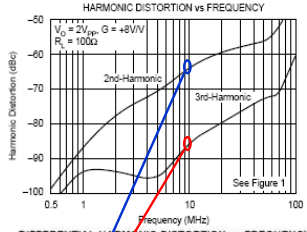


Texas Instruments

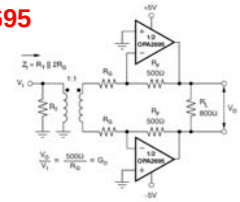
SE-Diff Performance Comparison: Dual Op amp with Input transformer

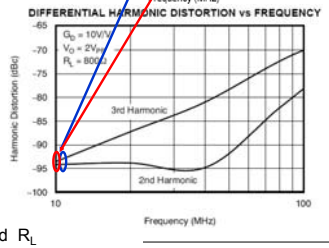
OPA695





OPA2695

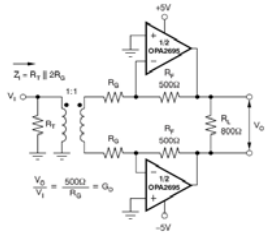


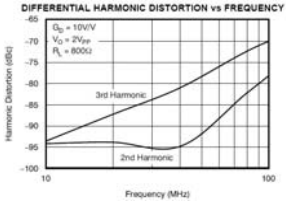


- 30dB improvement in HD2
- 7dB improvement in HD3 due to increased R_L

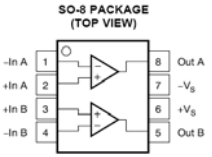
TEXAS INSTRUMENTS

OPA2695 with optimized package & pin-out





- Differential circuit architecture with nonstandard device pin-out optimized for signal path symmetry.
  - Attenuated HD2.
  - G = 20dB

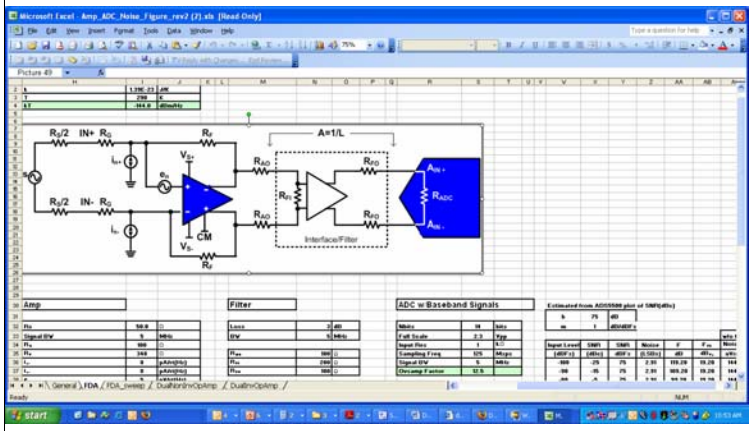


TEXAS INSTRUMENTS

Amp/ADC Applications Tools

- Application notes
- Spreadsheet tools
- Eval boards
  - Can be challenging to use individual amp/ADC EVM boards together.
    - EVMs usually emphasize the performance of individual devices.
    - Might not accurately reflect the total performance of the two devices that normally share one PCB.
- Will release a combined amp/ADC EVM in 4Q08.
  - TSW1070

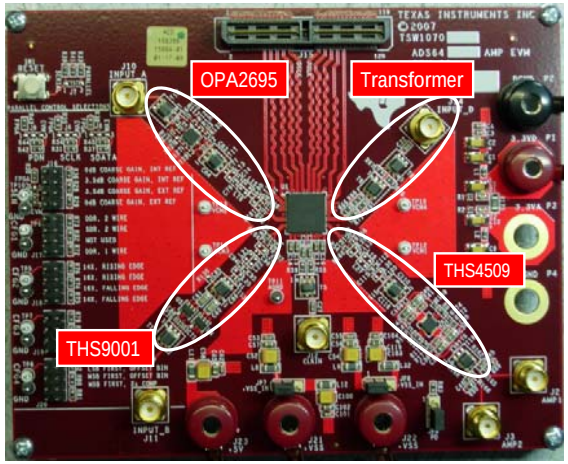
Spreadsheet Tool



TSW1070

Combined amplifier + ADC evaluation board for prototyping

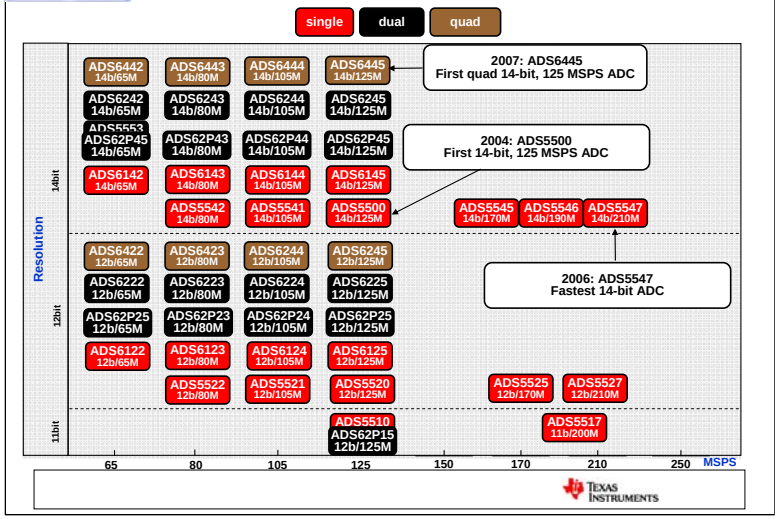
TSW1070 Top Side



TSW1070

- Goal
  - Provide a powerful, flexible, reliable solution for design & test of active, high-speed ADC interfaces.
- Featured devices
  - Quad 125MHz ADC: ADS6444
    - Sampling thru 2nd Nyquist zone.
    - Supporting narrowband & broadband applications
  - Three high-speed amplifiers:
    - THS4509, OPA2695, THS9001
  - Single passive interface w/transformer.
- Will be orderable w/supporting documentation.
  - Fully populated.
  - EVM user Guide
  - Application note(s).

ADS55xx/ADS6xxx High-Speed ADC Portfolio

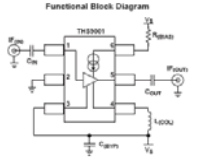


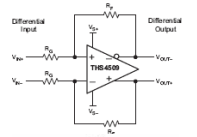
TSW1070 EVM Active Drivers

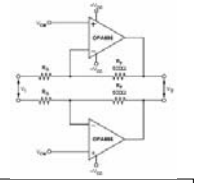
- THS9001 – G=15dB, RF/IF amplifier
  - Narrowband IF applications.

- THS4509 – Fully differential amplifier
  - — Voltage feedback
  - — Broadband & narrowband applications.
  - — AC-coupled & DC-coupled configurations

- OPA2695 - Dual current-feedback
  - Optimized for G = +8 operation.
  - Inverting or noninverting gain.
  - Broadband, high gain applications.
  - Silicon & pin-out optimized for differential operation.





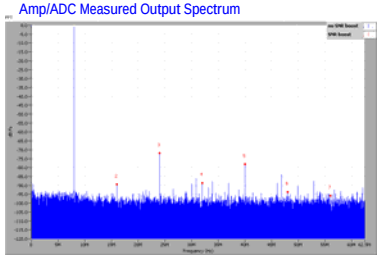


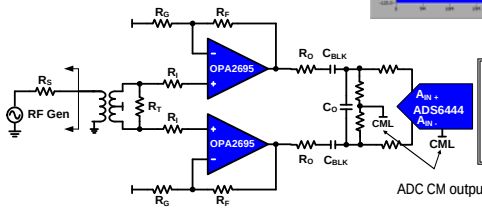
TEXAS INSTRUMENTS

OPA2695 Interface

- Basic circuit appears below.
  - High differential input impedance w/respect to device terminals
    - R_T, R_I to facilitate testing w/lab equipment.
    - For DC-coupled amp output, remove C_{BLK}, connect CML to R_G.
  - V_{SUPPLY} = 10V ⇒ 5V
  - Device optimized for G = +8V/V
    - CFB: BW weakly dependent on gain.
  - 14 bit operation to ~40MHz

Amp/ADC Measured Output Spectrum



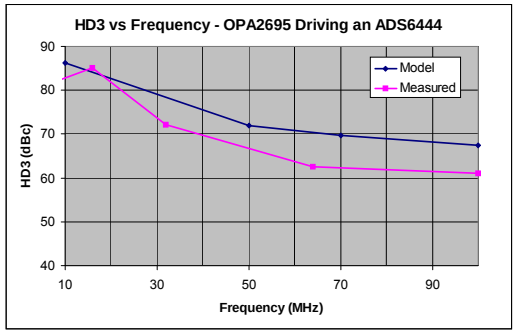


ADC CM output

Applications:
- Broadband Modems/Receivers
- High-Speed Instrumentation
- Transimpedance/sensors

OPA29695/ADS6444

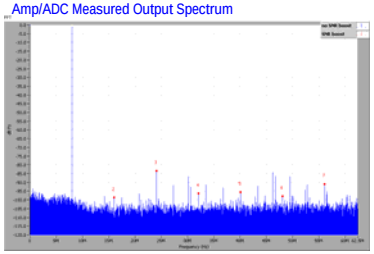
- Individual HD3 performance from device data sheets.
- Analysis for combined amp/ADC HD3 performance from earlier slides.
- Model is within 4dB-5dB of the measured results over the useful frequency range (10MHz-35MHz) for this application.

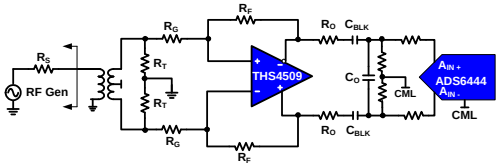


THS4509 Interface

- Basic circuit appears below.
  - Gain set by R_F/R_G.
    - Voltage-feedback device: BW & gain are inversely proportional.
    - Default values give G=10dB: R_F = 348Ω, R_G = 100Ω
    - R_T chosen to match amp input to test equipment
  - V_{SUPPLY} = 5V ⇒ 3V
  - 14 bit operation to ~50MHz, G=10dB
  - Can easily modify EVM to support:
    - Broadband, DC-coupled signal path
    - Narrowband, filtered path
    - Single-ended or differential inputs

Amp/ADC Measured Output Spectrum



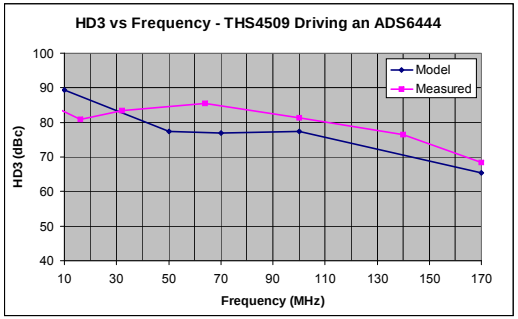


Applications:
- Radio/SDR
- Telemetry
- Ranging
- Test & Meas.
- Modems/Receivers

Texas Instruments

THS4509/ADS6444

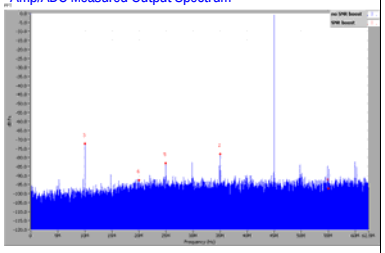
- Individual HD3 performance from device data sheets.
- Analysis for combined amp/ADC HD3 performance from earlier slides.
- Model is within 5dB-6dB over the useful frequency range (10MHz-60MHz) for this application.

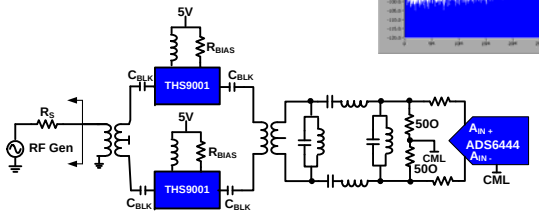


THS9001 Interface

- Basic circuit appears below.
  - Fixed Gain = 15dB
    - $R_{IN} = R_{OUT} = 50\Omega$
    - BW = 50MHz - 350MHz
    - IF/narowband applications
  - $V_{SUPPLY} = 5V \Rightarrow 3V$

Amp/ADC Measured Output Spectrum



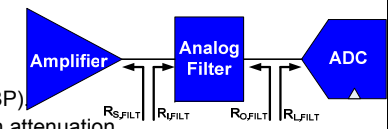


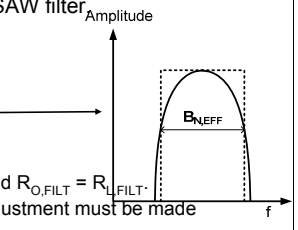
Applications:
- Radio/SDR
- Telemetry
- Ranging
- IF signal chain

Texas Instruments

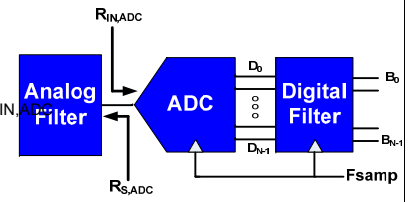
Analog Filter Parameters

- ADC anti-aliasing & input noise reduction.
  - Low-pass (LP) or band-pass (BP)
  - Modeled as a passive filter with attenuation. Often an RC low-pass, LC bandpass or SAW filter
- Signal and Noise Parameters
  - Loss = L = Pin/Pout = 1/Gp
  - BW = B < Fsamp/2
    - Equivalent noise BW
  - Noise
    - NF = L when L is measured for $R_{S,FILT} = R_{I,FILT}$ and $R_{O,FILT} = R_{L,FILT}$.
    - If $R_{S,FILT} \neq R_{I,FILT}$ or $R_{O,FILT} \neq R_{L,FILT}$, an adjustment must be made to the signal attenuation.





ADC Parameters



- ADC Input
  - Signal: $P_{SIG,IN} = (V_{FS,RMS})^2/R_{IN,ADC}$
  - Noise: $P_{N,IN} = 4kTBR_{O,FILT}$
- ADC Output
  - ADC output (SNR_{ADC}) is defined over the band $\{f_1,f_2\} = \{0, Fsamp/2\}$.
    - Signal BW = B
    - Output Noise BW = Fsamp/2
  - Digital filter bandlimits the output to BW = B.
    - The noise power is reduced by (*Fsamp/2B*).
  - The effective output: $SNR_{OUT,EFF} = SNR_{OUT,ADC} \cdot \underbrace{\frac{F_{SAMP}}{2B}}$

Oversampling Gain (Gos)

ADC Noise Factor

$$NF_{ADC} = \frac{SNR_{IN,ADC}}{SNR_{OUT,EFF}} = \underbrace{\frac{V_{FS,RMS}^2}{R_{S,ADC}}}_{\text{Max ADC Input Power}} \underbrace{\frac{1}{kTB}}_{\text{Thermal Noise Power}} \frac{SNR_{OUT,ADC}^{-1}}{\left(\frac{F_{SAMP}}{2B}\right)}$$

Nominal ADC Output SNR

Oversampling Gain (Gos)

- If the sampling frequency is very large relative to the signal BW (large oversampling gain) the NF_{ADC} can appear nearly as good as a high-performance amplifier.
- Backend blocks in signal chains usually have poor noise figure (see why in the next few slides).
- This can create a perception problem with our customers.