APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 present a few examples of typical applications of the 8255A.

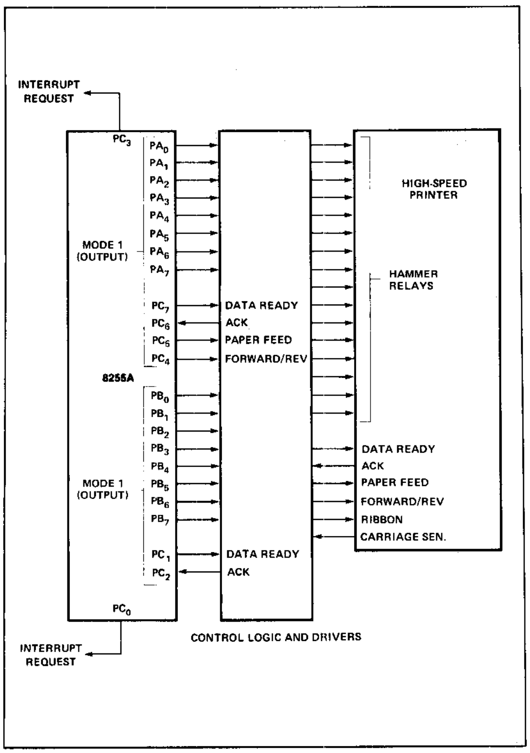


Figure 19. Printer Interface

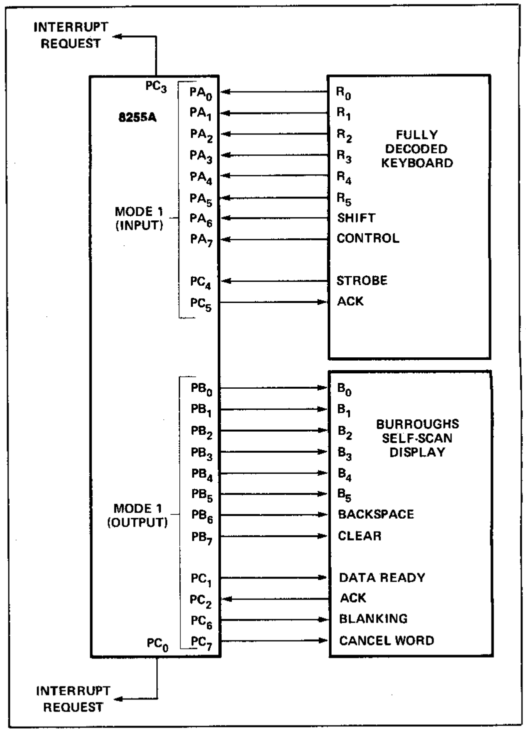


Figure 20. Keyboard and Display Interface

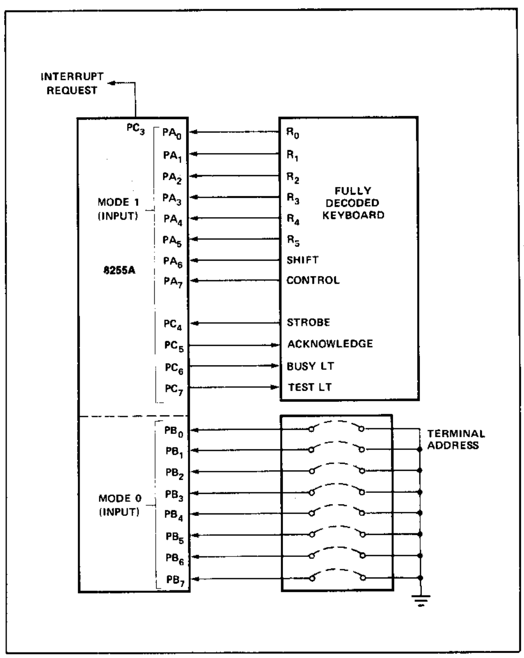


Figure 21. Keyboard and Terminal Address Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . –0.5V to +7V
Power Dissipation . . . . 1 Watt

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	I_{OL} = 2.5mA
V_{OL} (PER)	Output Low Voltage (Peripheral Port)		0.45	V	I_{OL} = 1.7mA
V_{OH} (DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH} (PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V

NOTE:
1. Available on any 8 pins from Port B and C.

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V)

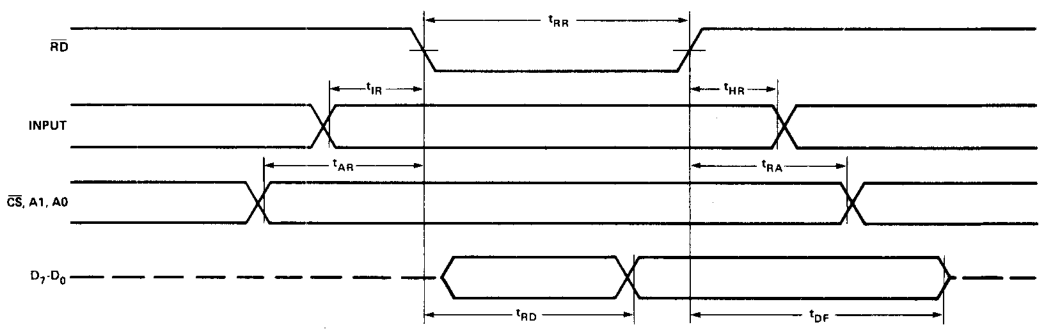
Bus Parameters

READ

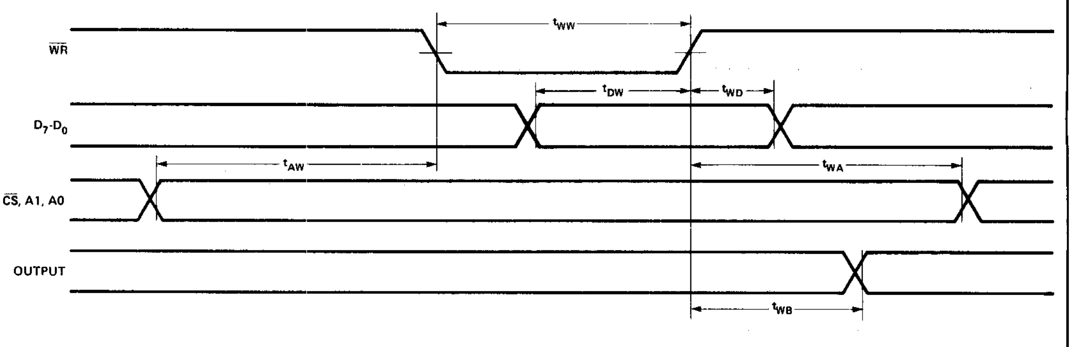
Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns

WAVEFORMS

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)



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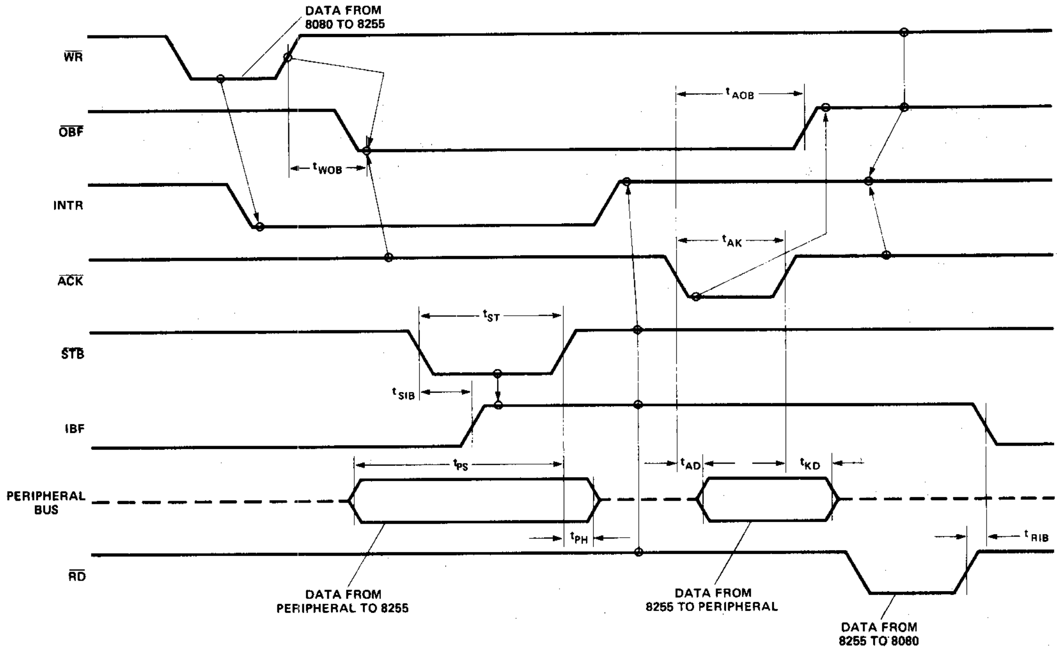
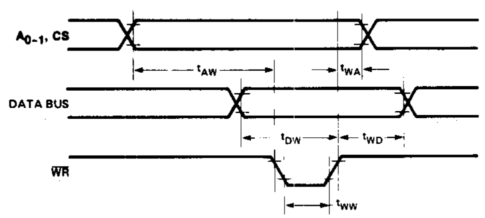
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)

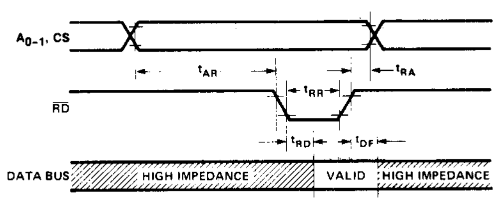


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

WRITE TIMING



READ TIMING



AFN-00744B

8256 MULTIFUNCTION UNIVERSAL ASYNCHRONOUS RECEIVER-TRANSMITTER (MUART)

- **Programmable Serial Asynchronous Communications Interface for 5-, 6-, 7-, or 8-Bit Characters, 1, 1½, or 2 Stop Bits, and Parity Generation**
- **On-Board Baud Rate Generator Programmable for 13 Common Baud Rates up to 19.2K Bits/second, or an External Baud Clock Maximum of 1M Bit/second**
- **Five 8-Bit Programmable Timer/Counters; Four Can Be Cascaded to Two 16-Bit Timer/Counters**
- **Two 8-Bit Programmable Parallel I/O Ports; Port 1 Can Be Programmed for Port 2 Handshake Controls and Event Counter Inputs**
- **Eight-Level Priority Interrupt Controller Programmable for 8085 or iAPX 86, iAPX 88 Systems and for Fully Nested Interrupt Capability**
- **Programmable System Clock to 1 ×, 2 ×, 3 ×, or 5 × 1.024 MHz**

The Intel® 8256 Multifunction Universal Asynchronous Receiver-Transmitter (MUART) combines five commonly used functions into a single 40-pin device. It is designed to interface to the 8048, 8085A, iAPX 86, and iAPX 88 to perform serial communications, parallel I/O, timing, event counting, and priority interrupt functions. All of these functions are fully programmable through nine internal registers. In addition, the five timer/counters and two parallel I/O ports can be accessed directly by the microprocessor.

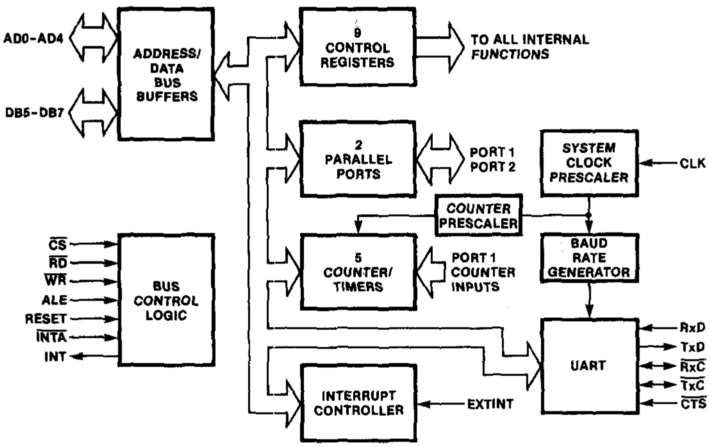


Figure 1. MUART Block Diagram

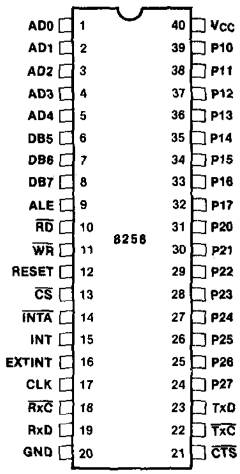


Figure 2. MUART Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
AD0-AD4 DB5-DB7	1-5 6-8	I/O	**Address/Data:** Three-State Address/Data lines which interface with the CPU lower 8-bit address/data bus. The 5-bit address is latched on the falling edge of ALE. In 8048 and 8085 mode, AD0-AD3 are used to select the proper register, while AD1-AD4 are used in 8086 and 8088 mode. The 8-bit bidirectional data bus is either written into or read from the chip depending on the latched $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$.
ALE	9	I	**Address Latch Enable:** Latches the 5 address lines on AD0-AD4 and $\overline{CS}$ on the falling edge.
$\overline{RD}$	10	I	**Read Control:** When this signal is low, the previously selected register is enabled onto the data bus.
$\overline{WR}$	11	I	**Write Control:** When this signal is low, the value on the data bus is placed into the previously selected register.
RESET	12	I	Pulse provided by the CPU to initialize the system. The MUART remains "idle" until it is reprogrammed by the CPU.
$\overline{CS}$	13	I	**Chip Select:** A low on this signal enables the MUART. It is latched with the address on the falling edge of ALE, and $\overline{RD}$ and $\overline{WR}$ have no effect unless $\overline{CS}$ was latched low during the ALE cycle.
$\overline{INTA}$	14	I	**Interrupt Acknowledge:** If the MUART has been enabled to respond to interrupts, it puts an RST on the bus for the 8085 or a vector for the 8086. The bit in the interrupt register is reset when the interrupt is placed onto the bus.
INT	15	O	**Interrupt:** A high signals the CPU that the MUART needs service.
EXTINT	16	I	**External Interrupt:** A high on this pin signals that an external device requests service. EXTINT must be held high until $\overline{INTA}$ or read interrupt occurs.
CLK	17	I	**System Clock:** This input provides an accurate timing source for the MUART. It must be 1×, 2×, 3×, or 5× 1.024 MHz and is used by the baud rate generator and real time clocks.
$\overline{RxC}$	18	I/O	**Receive Clock:** If baud rate 0 is selected, this input clocks bits into RxD on the rising edge. If a baud rate from 1-$0F_{16}$ is selected, this output will provide a rising edge at the center of each received data bit. This output remains high during start, stop, and parity bits.
RxD	19	I	**Receive Data:** Serial data input from the modem or terminal to the MUART.
GND	20	PS	**Ground:** Power supply and logic ground reference.

Symbol	Pin No.	Type	Name and Function
V_{CC}	40	PS	**Power:** +5V POWER supply.
P17-P10	32-39	I/O	**Parallel I/O Port 1:** Each pin can be programmed as an input or an output to perform general purpose I/O functions for the CPU under software control. In addition to general I/O, I/O Port 1 can be programmed to a variety of special functions for handshake control, counter inputs, and special communications functions.
P27-P20	24-31	I/O	**Parallel I/O Port 2:** Each nibble (4 bits) of this port can be either an input or an output. Also, this port can be used as a bidirectional 8-bit port using handshake lines in Port 1.
TxD	23	O	**Transmit Data:** This output carries the serial data to the terminal or modem from the MUART.
$\overline{TxC}$	22	I/O	**Transmit Clock:** If the baud rate is 0, this input clocks data out of the transmitter on the falling edge. If a baud rate of 1 or 2 is selected, this input permits the user to provide a 32× or 64× clock which is used for the receiver and transmitter. If the baud rate is 3-$0F_{16}$, the internal transmitter clock is output. If 1½ stop bits are selected and characters are continuously transmitted, the internal baud rate generator will be reset at the end of the stop bits and the clock will have a small positive spike instead of a half clock. A high-to-low transition occurs at the beginning of each bit and a low-to-high transition at the center of each bit.
$\overline{CTS}$	21	I	**Clear to Send:** This input enables the serial transmitter. If $\overline{CTS}$ is low, any character in the transmitter buffer will be sent. A single negative-going pulse causes the transmission of a single previously loaded character out of the transmitter buffer. If this pulse occurs when the buffer is empty or during the transmission of a character up to 0.5 of the first stop bit, it will be ignored. If a baud rate from 1-$0F_{16}$ is selected, $\overline{CTS}$ must be low for at least 1/32 of a bit, or it will be ignored.

FUNCTIONAL DESCRIPTION

The 8256 Multi-Function Universal Asynchronous Receiver-Transmitter (MUART) combines five commonly used functions onto a single 40-pin device. The MUART performs asynchronous serial communications, parallel I/O, timing, event counting, and interrupt control.

Serial Communications

The serial communications portion of the MUART contains a full-duplex asynchronous receiver-transmitter (UART). A programmable baud rate generator is included on the MUART to permit a variety of operating speeds without external components. The UART can be programmed by the CPU for a variety of character sizes, parity generation and detection, error detection, and start/stop bit handling. The receiver checks the start and stop bits in the center of the bit, and a break halts the reception of data. The transmitter can send breaks and can be controlled by an external enable pin.

Parallel I/O

The MUART includes 16 bits of general purpose parallel I/O. Eight bits (Port 1) can be individually changed from input to output or used for special I/O functions. The other eight bits (Port 2) can be used as nibbles (4 bits) or as bytes. These eight bits also include a handshaking capability using two pins on Port 1.

Counter/Timers

There are five 8-bit counter/timers on the MUART. The timers can be programmed to use either a 1 kHz or 16 kHz clock generated from the system clock. Four of the 8-bit counter/timers can be cascaded to two 16-bit counter/timers, and one of the 8-bit counter/timers can be reset to its initial value by an external signal.

Interrupts

An eight-level priority interrupt controller can be configured for fully nested or normal interrupt priority. Seven of the eight interrupts service functions on the MUART (counter/timers, UART), and one external interrupt is provided which can be used for a particular function or for chaining interrupt controllers or more MUARTs. The MUART will support 8085 and 8086/88 systems with direct interrupt vectoring, or the MUART can be polled to determine the cause of the interrupt.

Command Register 1

L1	L0	S1	S0	BRKI	BITI	8086	FRQ
	(0R)				(0W)		

FRQ — Timer Frequency Select

This bit selects between two frequencies for the five timers. If FRQ = 0, the timer input frequency is 16 kHz (62.5 μs). If FRQ = 1, the timer input frequency is 1 kHz (1 ms). The selected clock frequency is shared by all the counter/timers enabled for timing; thus, all timers must run with the same time base.

8086 — 8086 Mode Enable

This bit selects between 8048/8085 mode and 8086/8088 mode. In 8085 mode (8086 = 0), A0 to A3 are used to address the internal registers, and an RST instruction is generated in response to the first $\overline{INTA}$. In 8086 mode (8086 = 1), A1 to A4 are used to address the internal registers, and A0 is used as an extra chip select (A0 must equal zero to be enabled). The response to $\overline{INTA}$ is for 8086 interrupts where the first $\overline{INTA}$ is ignored, and an interrupt vector (40_{16} to 47_{16}) is placed on the bus in response to the second $\overline{INTA}$.

BITI — Interrupt on Bit Change

This bit disables the Timer 2 interrupt and enables an interrupt when a low-to-high transition occurs on pin 7 of Port 1 (pin 32).

BRKI — Break-In Detect Enable

This bit enables the break-in detect feature. A break-in is detected when pin 6 of Port 1 (pin 33) is low during the first stop bit of a transmitted character. This could be used to detect a break-in condition by connecting the serial transmission line to pin 33. A break-in detect is OR-ed with break detect in bit 3 of the Status Register. If $\overline{RxC}$ and $\overline{TxC}$ are used for the serial bit rates, break-in cannot be detected.

S0, S1 — Stop Bit Length

S1	S0	Stop Bit Length
0	0	1
0	1	1.5
1	0	2
1	1	0.75

If 0.75 stop bits is selected, $\overline{CTS}$ becomes edge sensitive rather than level sensitive. A high-to-low transition of $\overline{CTS}$ *immediately* initiates the transmission of the next character. A high-to-low transition will be ignored if the transmit buffer is empty, or if it occurs before 0.75 of the first stop bit. It will shorten the stop

Table 2. MUART Registers

Read Registers									8085 Mode: AD3 8086 Mode: AD4	AD2 AD3	AD1 AD2	AD0 AD1	Write Registers								
Command 1	L1	L0	S1	S0	BRKI	BITI	8086	FRQ	0	0	0	0	L1	L0	S1	S0	BRKI	BITI	8086	FRQ	Command 1
Command 2	PEN	EP	C1	C0	B3	B2	B1	B0	0	0	0	1	PEN	EP	C1	C0	B3	B2	B1	B0	Command 2
Command 3	0	RxE	IAE	NIE	0	SBRK	TBRK	0	0	0	1	0	SET	RxE	IAE	NIE	END	SBRK	TBRK	RST	Command 3
Mode	T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2C0	0	0	1	1	T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2C0	Mode
Port 1 Control	P17	P16	P15	P14	P13	P12	P11	P10	0	1	0	0	P17	P16	P15	P14	P13	P12	P11	P10	Port 1 Control
Interrupt Enable	L7	L6	L5	L4	L3	L2	L1	L0	0	1	0	1	L7	L6	L5	L4	L3	L2	L1	L0	Set Interrupts
Interrupt Address	D7	D6	D5	D4	D3	D2	D1	D0	0	1	1	0	L7	L6	L5	L4	L3	L2	L1	L0	Reset Interrupts
Receiver Buffer	D7	D6	D5	D4	D3	D2	D1	D0	0	1	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Transmitter Buffer
Port 1	D7	D6	D5	D4	D3	D2	D1	D0	1	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	Port 1
Port 2	D7	D6	D5	D4	D3	D2	D1	D0	1	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Port 2
Timer 1	D7	D6	D5	D4	D3	D2	D1	D0	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Timer 1
Timer 2	D7	D6	D5	D4	D3	D2	D1	D0	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Timer 2
Timer 3	D7	D6	D5	D4	D3	D2	D1	D0	1	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0	Timer 3
Timer 4	D7	D6	D5	D4	D3	D2	D1	D0	1	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Timer 4
Timer 5	D7	D6	D5	D4	D3	D2	D1	D0	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Timer 5
Status	INT	RBF	TBE	TRE	BD	PE	OE	FE	1	1	1	1	0	RS4	RS3	RS2	RS1	RS0	TME	DSC	Modification

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bit if it occurs after ¾ of the stop bit has been sent. If $\overline{CTS}$ is high or low or a low-to-high transition occurs, the transmitter remains idle.

L0, L1 — Character Length

L1	L0	Character Length
0	0	8
0	1	7
1	0	6
1	1	5

Command Register 2

PEN	EP	C1	C0	B3	B2	B1	B0

(1R) (1W)

B0, B1, B2, B3 — Baud Rate Select

B3	B2	B1	B0	Baud Rate	Sampling Rate
0	0	0	0	$\overline{TxC}$, $\overline{RxC}$	1
0	0	0	1	$\overline{TxC}$/64	64
0	0	1	0	$\overline{TxC}$/32	32
0	0	1	1	19200	32
0	1	0	0	9600	64
0	1	0	1	4800	64
0	1	1	0	2400	64
0	1	1	1	1200	64
1	0	0	0	600	64
1	0	0	1	300	64
1	0	1	0	200	64
1	0	1	1	150	64
1	1	0	0	110	64
1	1	0	1	100	64
1	1	1	0	75	64
1	1	1	1	50	64

If the baud rate is 0, then both the transmitter and receiver operate from separate external clocks. If the baud rate is 1 or 2, then both the transmitter and receiver divide the $\overline{TxC}$ by 64 or 32, respectively.

C0, C1 — System Clock Divider

C1	C0	Divider Ratio	System Clock Frequency
0	0	5	5.120 MHz
0	1	3	3.072 MHz
1	0	2	2.048 MHz
1	1	1	1.024 MHz

EP — Even Parity

If parity is enabled, then even parity is enabled by a 1 and odd parity is enabled by a 0.

PEN — Parity Enable

This enables parity detection and generation. The type of parity is determined by the EP bit.

Command Register 3

SET	RxE	IAE	NIE	END	SBRK	TBRK	RST

(2R) (2W)

Command Register 3 is different from the first two registers because it has a bit set/reset capability. Writing a byte with bit 7 high sets any bits which were also high. Writing a byte with bit 7 low resets any bits which were high. If any bit 0–6 is low, no change occurs to that bit. When Command Register 3 is read, bits 0, 3, and 7 will always be zero.

RST — Reset

If RST is set, the following events occur:

1. All bits in the Status Register except bits 4 and 5 are cleared, and bits 4 and 5 are set.
2. The Interrupt Enable, Interrupt Request, and Interrupt Service Registers are cleared.
3. The receiver and transmitter are reset. The transmitter goes idle (TxD is high), and the receiver enters start bit search mode.
4. If Port 2 is programmed for handshake mode, $\overline{IBF}$ and $\overline{OBF}$ are reset high.

RST does *not* alter ports, data registers or command registers, but it halts any operation in progress. RST is automatically cleared.

TBRK — Transmit Break

This causes the transmitter data to be set low, and it stays low until TBRK is cleared. As long as break is active, data transfer from the Transmitter Buffer to the Transmitter Register will be inhibited.

SBRK — Single Character Break

This causes the transmitter data to be set low for one character including start bit, data bits, parity bit, and stop bits. SBRK is automatically cleared when time for the last data bit has passed. It will start after the character in progress completes and will delay the next data transfer from the Transmitter Buffer to the Transmitter Register until TxD returns to an idle (marking) state. If both TBRK and SBRK are set, break will be sent as long as TBRK is set, but SBRK will be cleared after one character time of break. If SBRK is set again, it remains set for another character. The user can send a definite number of break characters in this manner by clearing TBRK after setting SBRK for the last character time.

END — End of Interrupt

If fully nested interrupt mode is selected, this bit resets the currently served interrupt level in the Interrupt Service Register. *This command must occur at the end of each interrupt service routine during fully nested* *interrupt mode.* END is automatically cleared when the Interrupt Service Register (internal) is cleared. See the NIE description for more information on nested interrupt servicing. END is ignored if nested interrupts are not enabled.

NIE — Nested Interrupt Enable

This bit enables fully nested interrupts. In this mode, the service routine for a lower priority interrupt can be interrupted by a request from a higher priority task.

In fully nested interrupt mode, $\overline{INTA}$ or reading the Interrupt Address Register resets the highest priority interrupt bit in the Interrupt Register (internal), sets the corresponding bit in the Interrupt Service Register (internal), and resets INT. If an interrupt of higher priority than the currently served interrupt is requested or the END bit is set while another interrupt request is pending, the INT line will go high again. If an interrupt service routine is interrupted by an interrupt of higher priority, two or more bits in the Interrupt Service Register will be set.

If NIE is low, interrupt priority is used only when two interrupts occur at the same time. INT will be high as long as the CPU has not responded to all the interrupts in the Interrupt Register.

IAE — Interrupt Acknowledge Enable

This bit enables an automatic response to $\overline{INTA}$. The particular response is determined by the 8086 bit in Command Register 1.

RxE — Receiver Enable

This bit enables the serial receiver. The Receiver Buffer and all receiver status information will be disabled except for the break detect status.

SET — Bit Set/Reset

If this bit is high during a write to Command Register 3, then any bit marked by a high will be set. If this bit is low, then any bit marked by a high will be cleared.

Mode Register

T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2C0

(3R) (3W)

P2C2, P2C1, P2C0 — Port 2 Control

				Direction	
P2C2	**P2C1**	**P2C0**	**Mode**	**Upper**	**Lower**
0	0	0	nibble	input	input
0	0	1	nibble	input	output
0	1	0	nibble	output	input
0	1	1	nibble	output	output
1	0	0	byte handshake	input	
1	0	1	byte handshake	output	
1	1	0	*DO NOT USE*		
1	1	1	test		

If test mode is selected and BRG of Port 1 Control Register is set, then the output from the internal baud rate generator is placed on pin 4 of Port 1 (pin 35).

CT2, CT3 — Counter/Timer Mode

If CT2 or CT3 are high, then counter/timer 2 or 3 respectively is configured as an event counter on pin 2 or 3 respectively of Port 1 (pins 37 or 36). The event counter decrements the count by one on each low-to-high transition of the external input. If CT2 or CT3 is low, then the respective counter/timer is configured as a timer and the Port 1 pins are used for parallel I/O.

T5C — Timer 5 Control

If T5C is set, then Timer 5 can be preset and started by an external signal. Writing to the Timer 5 Register loads the Timer 5 Save Register and stops the timer. A high-to-low transition on pin 5 of Port 1 (pin 34) loads the timer with the saved value and starts the timer. The next high-to-low transition on pin 5 retriggers the timer by reloading it with the initial value and continues timing.

When the timer reaches zero it issues an interrupt request, disables its interrupt level and continues counting. A subsequent high-to-low transition on pin 5 resets Timer 5 to its initial value. For another timer interrupt, the Timer 5 interrupt enable bit must be set again.

T35, T24 — Cascade Timers

These two bits cascade Timers 3 and 5 or 2 and 4. Timers 2 and 3 are the lower bytes, while Timers 4 and 5 are the upper bytes. If T5C is set, then both Timers 3 and 5 can be preset and started by an external pulse. When a high-to-low transition occurs, Timer 5 is preset to its saved value, but Timer 3 is always preset to all ones. If either CT2 or CT3 is set, then the corresponding timer pair is a 16-bit event counter.

Port 1 Control Register

P17	P16	P15	P14	P13	P12	P11	P10

(4R) (4W)

Each bit in the Port 1 Control Register configures the direction of the corresponding pin. If the bit is high, the pin is an output, and if it is low the pin is an input. Every Port 1 pin has another function which is controlled by other registers. If that special function is disabled, the pin functions as a general I/O pin as specified by this register. The special functions for each pin are described below.

Port 10, 11 — Handshake Control

If byte handshake control is enabled for Port 2 by the Mode Register, then Port 10 is programmed as $\overline{STB}/\overline{ACK}$ handshake control input and Port 11 is programmed as $\overline{IBF}/\overline{OBF}$ handshake control output.

If byte handshake mode is enabled for output on Port 2, $\overline{OBF}$ indicates that a character has been loaded into the

Port 2 output buffer. When an external device reads the data, it acknowledges this operation by driving $\overline{ACK}$ low. $\overline{OBF}$ is set low by writing to Port 2 and is reset high by $\overline{ACK}$.

If byte handshake mode is enabled for input on Port 2, $\overline{STB}$ is an input to the MUART to latch the data into Port 2. After the data is latched, $\overline{IBF}$ is driven low. $\overline{IBF}$ is reset high when Port 2 is read.

Port 12, 13 — Counter 2, 3 Input

If Timer 2 or Timer 3 is programmed as an event counter by the mode register, then Port 12 or 13 is the counter input for Event Counter 2 or 3, respectively.

Port 14 — Baud Rate Generator Output Clock

If test mode is enabled by the Mode Register and Command Register 2 baud rate select is greater than 2, then Port 14 is an output from the internal baud rate generator.

Port 15 — Timer 5 Trigger

If T5C is set in the Mode Register enabling a retriggerable timer, then Port 15 is the input which starts and reloads Timer 5.

Port 16 — Break-In Detect

If break-in detect is enabled by BRKI in Command Register 1, then this input is used to sense a break-in. If Port 16 is low while the serial transmitter is sending the last stop bit, then a break-in condition is signaled.

Port 17 — Port Interrupt Source

If BITI in Command Register 1 is set, then a low-to-high transition on Port 17 generates an interrupt request on priority level 1.

Receiver and Transmitter Buffer

D7	D6	D5	D4	D3	D2	D1	D0

(7R) (7W)

Both the transmitter and the receiver in the MUART are fully double buffered. The Receiver Buffer full flag is cleared when the character is read. If the character is not read before the next character's first stop bit, then an overrun error is generated. Bytes written to the Transmitter Buffer are held until the Transmitter Register (internal) is empty. If the Transmitter Register is empty, the byte is transferred immediately and the Transmitter Buffer empty flag is set. If a serial character length is less than 8 bits, then the unused most significant bits are set to zero on a read and are ignored on a write.

Port 1

D7	D6	D5	D4	D3	D2	D1	D0

(8R) (8W)

Writing to Port 1 sets the data in the Port 1 output latch. Writing to an input pin does not affect the pin, but the data is stored and will be output if the direction of the pin is changed later. If the pin is used as a control signal, the pin will not be affected, but the data is stored. Reading Port 1 transfers the data in Port 1 onto the data bus. Reading an output pin or a control pin puts the data in the output latch (*not* the control signal) onto the data bus.

Interrupt Enable Register

L7	L6	L5	L4	L3	L2	L1	L0

(5R) (5W = enable, 6W = disable)

Interrupts are enabled by writing to the Set Interrupts Register (5W). Interrupts are disabled by writing to the Reset Interrupts Register (6W). Each bit set by the Set Interrupts Register (5W) will enable that level interrupt, and each bit set in the Reset Interrupts Register (6W) will disable that level interrupt. The user can determine which interrupts are enabled by reading the Interrupt Enable Register (5R).

Priority		Source
Highest	L0	Timer 1
	L1	Timer 2 or Port Interrupt
	L2	External Interrupt (EXTINT)
	L3	Timer 3 or Timers 3 & 5
	L4	Receiver Interrupt
	L5	Transmitter Interrupt
	L6	Timer 4 or Timers 2 & 4
Lowest	L7	Timer 5 or Port 2 Handshaking

Port 2

D7	D6	D5	D4	D3	D2	D1	D0

(9R) (9W)

Writing to Port 2 sets the data in the Port 2 output latch. Writing to an input pin does not affect the pin, but it does store the data in the latch. Reading Port 2 puts the input pins onto the bus or the contents of the output latch for output pins.

Timer 1-5

D7	D6	D5	D4	D3	D2	D1	D0

($0A_{16}$-$0E_{16}$ R) ($0A_{16}$-$0E_{16}$ W)

Reading Timer N puts the contents of the timer onto the data bus. If the counter changes while $\overline{RD}$ is low, the value on the data bus will not change. If two timers are cascaded, reading the high order byte will cause the low order byte to be latched. Reading the low order byte will unlatch them both. Writing to either timer or de-cascading them also clears the latch condition. Writing to a timer sets the starting value of that timer. If two timers are cascaded, writing to the high order byte presets the low order byte to all ones. Loading only the high order byte with a value of X leads to a count of $X \cdot 256 + 255$. Timers count down continuously. If the interrupt is enabled, it occurs when the counter changes from 1 to 0. When the interrupt is set in the Interrupt Register, interrupts are disabled in the Interrupt Mask Register.

Status Register

INT	RBF	TBE	TRE	BD	PE	OE	FE

($0F_{16}$ R)

FE — Framing Error, Transmission Mode

If transmission mode is disabled (in Modification Register), then FE indicates a framing error. A framing error is detected during the *first* stop bit. The error is reset by reading the Status Register or by a chip reset. A framing error does not inhibit the loading of the Receiver Buffer. If RxD remains low, the receiver will assemble the next character. The false stop bit is treated as the next start bit, and no high-to-low transition on RxD is required to synchronize the receiver.

If transmission mode is enabled, then this bit is used to suggest the transmitter was sending. FE will be high if the transmitter is active during the reception of the parity bit (or last data bit for no-parity). It is reset if the transmitter is not active or by a chip reset. The bit is intended to imply that the received character is from the transmitter in half-duplex systems.

OE — Overrun Error

If the user does not read the character in the Receiver Buffer before the next character is received and transferred to this register, then the OE bit is set. The OE flag is set during the reception of the first stop bit and is cleared when the Status Register is read or when a chip reset occurs.

PE — Parity Error

A parity error is set during the first stop bit and is reset by reading the Status Register or by a chip reset.

BD — Break Detect, Break-In Detect

If BRKI in Command Register 1 is set to enable break-in detect, then BD indicates a break-in condition. If Port 16 is low during the transmission of the last stop bit, then BD will be set near the end of the last stop bit. Break-in detect can only be detected if the internal baud rate generator is used. Break-in remains set until the Status Register is read or the chip is reset.

If BRKI is low, then BD indicates a break condition on the receiver. BD is set when the first stop bit of a break is sampled and will remain set until the Status Register is read or the chip is reset. The receiver will remain idle until the next high-to-low transition on RxD. A detected break inhibits the loading of the Receiver Buffer.

TRE — Transmitter Register Empty

This status bit indicates that the Transmitter Register is busy. It is set by a chip reset and when the last stop bit has left the transmitter. It is reset when a character is loaded into the Transmitter Register. If $\overline{CTS}$ is low, the Transmitter Register will be loaded during the transmission of the start bit. If $\overline{CTS}$ is high at the end of a character, TRE will remain high and no character will be loaded into the Transmitter Register until $\overline{CTS}$ goes low. If the transmitter was inactive before a character is loaded into the Transmitter Buffer, the Transmitter Register will be empty temporarily while the buffer is full. However, the data in the buffer will be transferred to the transmitter register immediately and TRE will be cleared while TBE is set.

TBE — Transmitter Buffer Empty

TBE indicates the Transmitter Buffer is empty and is ready to accept a character. TBE is set by a chip reset or the transfer of data to the Transmitter Register and is cleared when a character is written to the transmitter buffer.

RBF — Receiver Buffer Full

RBF is set when the Receiver Buffer has been loaded with a new character during the sampling of the first stop bit. RBF is cleared by reading the receiver buffer or by a chip reset.

INT — Interrupt Pending

The INT bit reflects the state of the INT pin (pin 15) and indicates an interrupt is pending in the Interrupt Register. It is reset by $\overline{INTA}$ or by reading the Interrupt Address Register if only one interrupt is pending and by a chip reset.

FE, OE, PE, RBF, and break detect all generate a level 4 interrupt when the receiver samples the first stop bit. TRE, TBE, and break-in detect generate a level 5 interrupt. TRE generates an interrupt when TBE is set and the Transmitter Register finishes transmitting. The break-in detect interrupt is issued at the same time as TBE or TRE.

Modification Register

0	RS4	RS3	RS2	RS1	RS0	TME	DSC

($0F_{16}$ W)

DSC — Disable Start Bit Check

DSC disables the receiver's start bit check. In this state the receiver will not be reset if RxD is not low at the center of the start bit. This function is disabled by a chip reset.

TME — *Transmission Mode Enable*

TME enables transmission mode and disables framing error detection. A chip reset disables transmission mode and enables framing error detection.

RS0, RS1, RS2, RS3, RS4 — Receiver Sample Time

The number in RSn alters when the receiver samples RxD. A chip reset sets this value to 0 which is the center of the bit (sample time = 16). The receiver sample time can be modified only if the receiver is *not* clocked by $\overline{RxC}$.

				Sample Time	
RS4	**RS3**	**RS2**	**RS1**	**RS0 = 0**	**RS0 = 1**
0	1	1	1	2	1
0	1	1	0	4	3
0	1	0	1	6	5
0	1	0	0	8	7
0	0	1	1	10	9
0	0	1	0	12	11
0	0	0	1	14	13
0	0	0	0	16	15
1	1	1	1	18	17
1	1	1	0	20	19
1	1	0	1	22	21
1	1	0	0	24	23
1	0	1	1	26	25
1	0	1	0	28	27
1	0	0	1	30	29
1	0	0	0	32	31

AFN-01498B