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Burroughs

Application Notes

SELF-SCAN® PANEL DISPLAYS

TIMING REQUIREMENTS

This Note Covers Single Register SELF-SCAN Panels with 111 Active Columns.

INTRODUCTION

This technical memorandum discusses the timing requirements of SELF-SCAN panel displays. The operation of SELF-SCAN panel displays is based on the principle of glow discharge and includes within the same device the sequential addressing function as well as the time shared dot matrix display function. A better understanding of the timing requirement of these displays will facilitate their application within existing system constraints.

The SELF-SCAN display can be thought of as incorporating two distinctly separate functions. One of these is the sequential addressing function, and the other is the display function. In discussing the timing requirements a similar distinction can be made.

ADDRESS TIMING

The addressing of individual columns in a SELF-SCAN display takes place on the scan or rear side of the panel. This sequential addressing is initiated by resetting the glow discharge to one extreme of the panel. This is done by applying a negative waveform to the reset cathode and thus establishing a column of 7 individual gas discharge areas on the scan side of this electrode. Then by sequentially energizing the 3 busses corresponding to the 3 phases, this column of gas discharge areas can be propagated from the reset cathode to cathode number 1, then cathode number 2, and so on, until the opposite extreme of the panel has been reached. This scan cycle is then repeated 60 or more times per second by energizing the reset cathode every time a new scan cycle is initiated.

SCAN PERIOD

The SELF-SCAN panel display specifications call out certain time limits for energizing the scan side of any given cathode. These limits are established with the assumption that the duty cycle remains constant by always scanning through all existing cathodes. In case of the standard 16/18 digit display panel there are 111 cathodes plus the reset cathode. The time of energizing any given cathode will be designated by the letter T.

The reset period, the time during which the reset cathode only is at ground level, is defined as T_R. In many applications $T_R = T$.

The upper limit of T is determined by the lowest possible scanning rate consistent with a flicker free display. This is given by the formula $f = \frac{1}{T \times N}$ where N is the number of cathodes in a display. For a scanning rate of 60 scans per second and a display having 111+1 cathodes, N = 112, the maximum period $T \simeq 150$ microseconds.

The low limit of period T is determined by the decay time of the metastables[1] in the gas. The phenomenon that limits the minimum period T can best be explained by a reference to Figure 1. Let us assume that the glow exists on the scan side of cathode number 4 which implies that Phase 1 is active. In normal operation, Phase 2 would be activated during a subsequent period T_2 which would cause the glow to step to cathode number 5. At the beginning of the next period T_3 the glow would step to cathode number 6. During the periods T_2 and T_3 the metastables associated with the cavities on the scan side of cathode number 4 have been decaying. At the initiation of period T_4, when Phase 1 is again energized, the concentration of metastables along cathode number 4 is not zero but it is nevertheless lower than the concentration of metastables in the cavities along cathode number 7. This differential in the concentration of metastables assures that the glow will step from cathode number 6 to cathode number 7 and the cells along cathode number 4 will not ionize. However, if the period T is reduced below a certain minimum, then in the above example Phase 1 becomes re energized much more rapidly. This shorter period of time between the

[1] Metastables are gas atoms that have been raised to an intermediate energy level from which they cannot return to the ground state without interacting with other particles. If this interaction takes place with an atom of lower ionization energy then the metastable causes this other atom to ionize. In the SELF-SCAN panel display the metastables of the neon ionize the atoms of an additive gas upon collision.

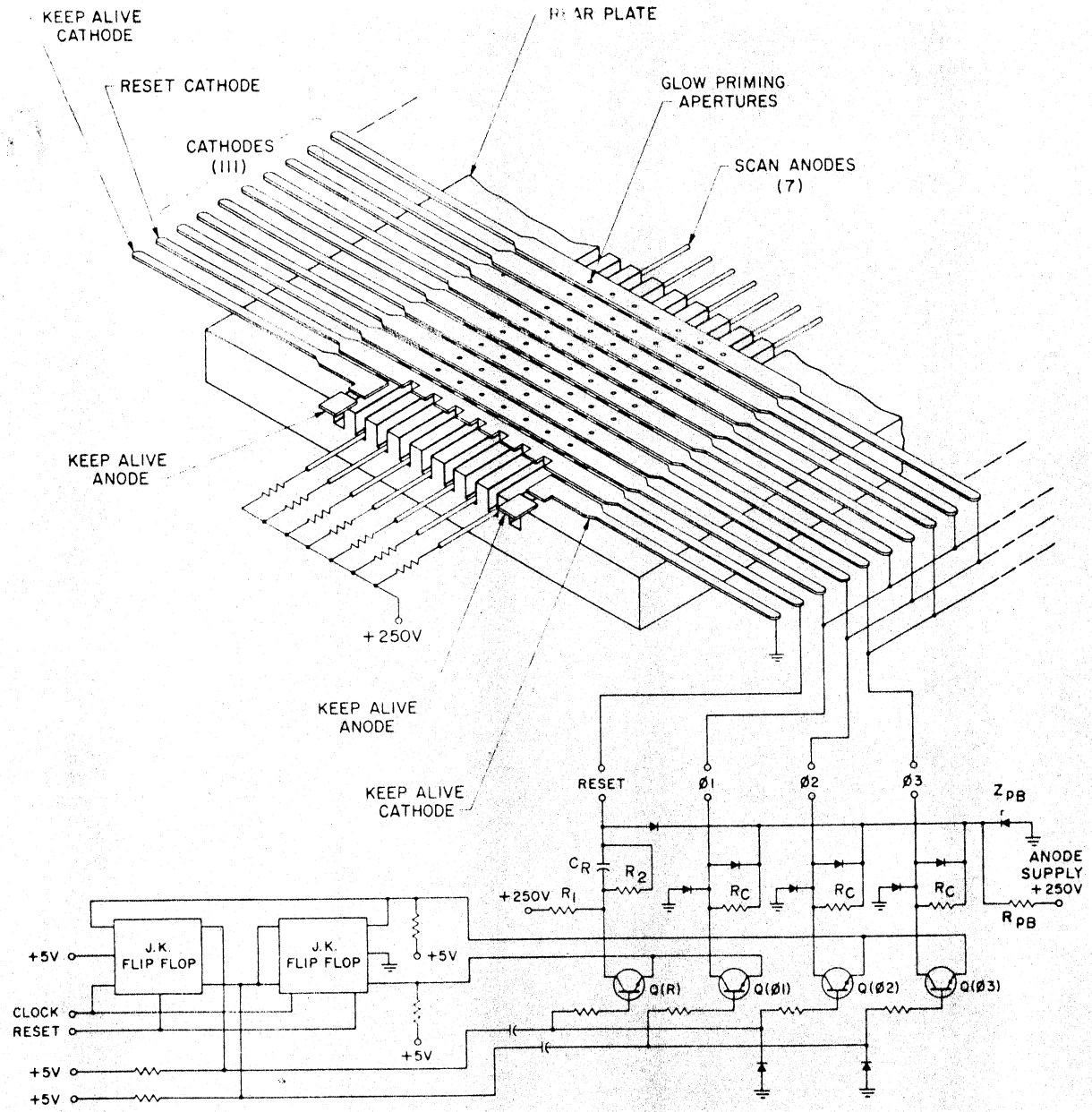

Figure 1. GLOW SCAN PORTION OF PANEL WITH TYPICAL ELECTRONICS
(For Recommended Component Values See Table 2)

re-energizing of the same phase does not allow sufficient differential in metastable concentration to develop which can in turn lead to the ionization of the wrong cells. In the above example, the glow instead of propagating from cathode 6 to cathode 7 may re-establish itself on cathode 4. If this takes place in a certain area of the panel repeatedly, it may exhibit itself as a much brighter three column segment on the scan side of these cathodes. In order to allow for some operating margins on voltages and on panel characteristics, the minimum limit on the period T is established somewhat above the actual operating limit of the panel.

RESET PERIOD

The limits on the reset time T_R are established on the basis of a different set of considerations. The reset cathode is not used for display purposes. Its only function is to re-establish the glow at the reset end of the panel. Therefore, the entire reset time T_R can be utilized for this purpose. Because of the proximity of two constantly energized keep-alive cells, the time required to reset the glow is relatively short. For circuit timing conveniences it is usually desirable to have $T_R = T$. To assure reliable resetting under such minimum time conditions, the reset cathode is generally pulsed to a more negative voltage than the remaining cathodes. The application of such over voltage has the effect of reducing the reset time.

If the reset period T_R were reduced below the value T, the reliability of resetting would be jeopardized. This means that occasionally the panel would not reset which would result in a recycling of the scan at the opposite extreme of the panel over the last three cathodes.

It is now obvious from the above discussion that increasing the reset period T_R makes resetting easier and more reliable. However, this has some undesirable consequences. If the reset time, $T_R = 2T$, then the reset cathode will always be stressed twice as much as any of the other cathodes. Since the reset cathode is not used for display, such additional stress is permissible. On the basis of test data the upper limit for a reset

period T_R has been established as $T_R = 3T$. This condition still does not produce a stress level that would significantly affect the life of the panel. It is generally true that by utilizing a longer reset period such as $T_R = 3T$, the over-voltage normaliy applied to the reset cathode can be reduced to 0. This means that the panel can be reset by merely grounding the reset cathode.

PHASE TIMING OVERLAP

Figure 2 is a timing diagram indicating the gross timing requirements for a 16 digit SELF SCAN panel display. Figure 2 does not indicate clearly whether there is any requirement for overlap between subsequent phase intervals.

The glow transfer phenomenon is by definition dependent on the existence of ionization on one cathode and its transfer to an adjacent cathode. For this reason there should be no delay between the termination of pulse T_N and the leading edge of the pulse T_{N+1} on the subsequent cathode. Although most panels would probably continue to operate with delays between T_N and T_{N+1} of up to a couple of microseconds, operating margins would be seriously reduced. The reason is that when the N cathode is de-energized there is a rapid decrease in the concentration of electrons and ions leaving only the metastables to initiate the ionization on the N+1 cathode. A much more desirable condition is obtained when the above described delay is 0. In typical circuits a few microseconds of timing overlap is common. Such a small timing overlap is not undesirable. Best operation is achieved when this overlap is within the range of 0 to 3 microseconds.

Excessive overlap of these signals may also be undesirable. Glow transfer may not take place until the previously energized cathode is returned to the positive bias voltage. During the period of timing overlap a glow transfer uncertainty takes place. During this period of transfer uncertainty the display anode must be inhibited and therefore the duty cycle and the brightness are reduced. Further reasons for inhibiting the display anodes during glow transfer are discussed under Display Timing.

DISPLAY TIMING

To accomplish glow transfer on the scan side from one cathode to an adjacent cathode requires a finite period of time in the order of one or more microseconds.

Once the glow is transferred to the adjacent cathode on the scan side, an additional delay is incurred before the display cavities become primed. This delay is due to the slow process of priming by means of diffusion of metastables through the small priming apertures.

In summary then, there are three distinct delays from the initiation of glow transfer until the new cathode display cavities are fully primed. One of these delays is the glow transfer uncertainty due to the overlap of phase signals. The second delay is due to the actual transfer of glow discharge to the adjacent cathode. The third delay is the priming of the display cell. During the time that these three processes are taking place the display anodes must be blanked. The blanking period required is usually in the order of a 10 to 20 microsecond.

If such blanking of the display anodes does not take place, malfunction may be observed in at least one of two ways. One of these may be evidenced as a ghost effect whereby display cavities associated with the N cathode become energized with the information intended for the N+1 cavities. The reason for this is that the display anode information becomes available prior to the actual glow transfer on the scan side of the panel.

Another malfunction that may occur in the absence of display anode blanking is the hanging up of the scan in a certain part of the panel under certain message conditions. This means that the panel begins to recycle over the range of three adjacent cathodes in some region of the panel. To illustrate how this can happen we will take a specific example and refer to Figure 1. Let us assume that the glow existed on the scan side of cathode number 3, but none of the display cavities associated with cathode number 3 were required to be energized for the given message. On the other hand, for the same message several display cavities along cathode number 2 and cathode number 1 were energized during the time period T_2 and T_1. The glow is now stepped on the scan side from cathode number 3 to cathode number 4 and the given message now requires the display of certain dots along cathode number 4, therefore, the anodes associated with these cavities are allowed to go positive. However, at the time that these display anodes go positive, the actual glow transfer and the priming of the display cells along cathode number 4 has not yet taken place. Consequently, the display cells along cathode number 4 cannot ionize for several microseconds until priming takes place from the scan side. On the other hand, some of the display cavities along cathode number 1 may still be primed at a low level since they were actually sustaining a glow discharge

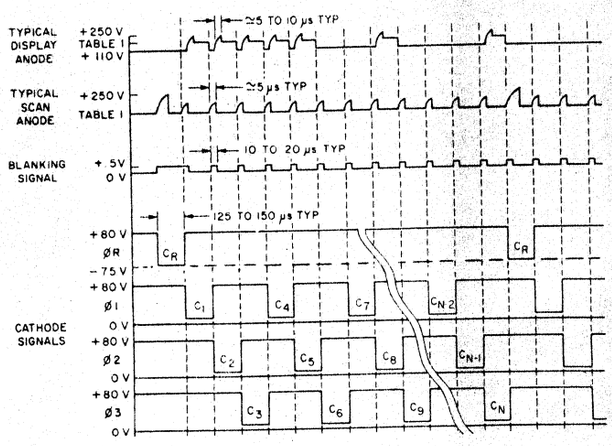

Figure 2. TIMING DIAGRAM

Description	Min	Nom	Max	Units
Display Anode Supply Voltage	237.5	250	262.5	Volts
Logic Voltage	4.75	5.0	5.25	Volts
Prebias Voltage	76	80	84	Volts
Display Anode Hold Off Voltage	100		120	Volts
Display Anode Sustaining Voltage		170		Volts
Scan Anode Sustaining Voltage		160		Volts
Scan Anode Current		.5		ma
Display Anode Current		1.3	1.5	ma

Table 1. TYPICAL OPERATING CONDITIONS

CAUTION

The clock should not be allowed to stall in any column for more than 50 milliseconds. Times longer than this can cause permanent damage to the particular column in which stalled. Prolonged energizing of a given column can cause heating and eventual cracking of the display at this location. Figure 1 shows one method to prevent the above condition from occurring. This consists of the flip-flops being capacitively coupled to the cathode driver. Failure of a clock signal for any time greater than that prescribed will cause loss of bias on the cathode transistors and loss of power to the cathodes.

Component Designation	Typical Value	Units	Power Rating
R_1	200K	Ω	¼W
R_2	160K	Ω	¼W
R_C	100K	Ω	¼W
R_{PB}	75K	Ω	½W
C_R	02	uf	200V
Z_{PB}	80	Volt	1W

Table 2. RECOMMENDED COMPONENT VALUES

merely 2T periods earlier. Therefore, these display cavities along cathode number 1 are still primed considerably more than the yet unprimed display cells along cathode number 4.

Since both cathode number 1 and number 4 are connected to the same buss which is presently held at ground potential, there will be a strong tendency for the display cells along cathode number 1 to ionize prior to ionization of display cells along cathode number 4. However, once these display cells along cathode number 1 fire, they cause priming of the scan side of cathode number 1.

At this point some combination of three phenomena will take place. (1) Some of the display cavities along cathode number 1 ionize whereas the corresponding display cavities along cathode number 4 should be ionizing. (2) The priming from the display side may cause the scan side of cathode number 1 to ionize at the same time that glow exists on the scan side of cathode number 4. This causes a malfunction of the scan cycle. (3) If the scan side of cathode number 1 does not ionize at the same time that the scan side of cathode number 4 is ionized, there may be sufficient priming particles diffusing to cathode number 2 to cause ionization of the scan side of cathode number 2 during the subsequent time period. This also represents a malfunction of the scan cycle since cathode number 5 should be ionized on the scan side during this time period.

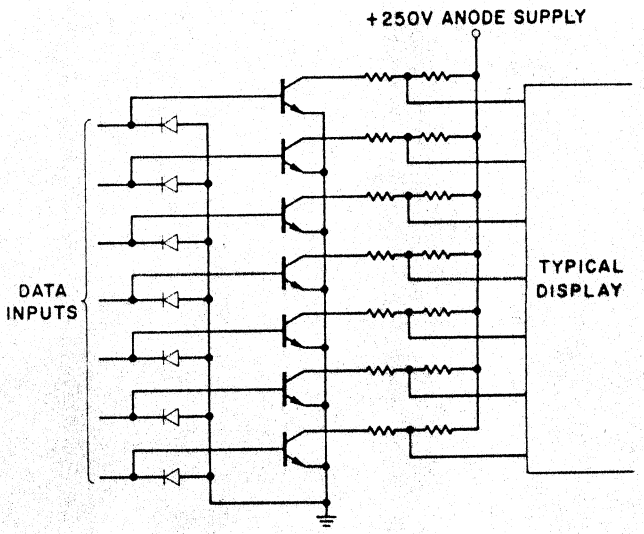

Figure 3. A TYPICAL DISPLAY ANODE DRIVE CIRCUIT

These reasons dictate the inhibiting of the display anodes for a period of time during the glow transfer process. Normally a 15 usec. inhibit time is sufficient. It is also necessary to inhibit the display anodes during the reset phase. There is no display capability during reset and any attempt to do so will cause a misscan.

For further information, write to Burroughs Corporation, Electronic Components Division, P. O. Box 1226, Plainfield, New Jersey 07061; or call our special sales/applications number, (201) 757-5000 in New Jersey, or (714) 835-7335 in California. For overseas inquiries, write to Burroughs ECD International, 11-15 Betterton Street, Drury Lane, London WC 2H 9BS England, Tel. 01-240-1479.

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